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Data Sheet

NT35510-Application Notes-HYDIS

One-chip Driver IC
with internal GRAM
for 16.7M colors 480RGB x 864 a-Si TFT LCD
with CPU / RGB / MIPI / MDDI Interface
or
without internal GRAM
for 16.7M colors 480RGB x 1024 a-Si TFT LCD
with RGB Interface

V0.07

Preliminary

REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Original	Kevin	SW	Dennis	2010/3/16
0.01	1. Add detail description for Page 0 Register (Command) 2. Add detail description for Page 1 Register (Command) 3. Add maximum series resistance section 4. Add timing example section	Kevin	SW	Dennis	2010/3/25
0.02	1. Page 0 Command Modification 0xB1(bits CGM removed, N565, RGBBP update, Add TE_PWR_SEL, DIS_EoTP_HS, removed CREV) 0xB4(Add vivid color function) 0xB5(Add 480RGB x 360) 0xB6(Add source data hold time) 0xB7(EQ function for GOA Ctrl signal) 0xB9(Source/VCOM Ctrl in non-display area) 0xBA(0xBB move to 0xBA, Source/VCOM/Gate Ctrl in V porch) 0xBB(0xBC move to 0xBB, Bias current) 0xBC(0xB8 move to 0xBC, inversion type) 0xBD-0xBF(update default value and T1/VBPD/VFPD description) 0xCC(Display timing update, also rename CLW to CLW_H,FTI to FTI_H) 0xD0(Add bit CLED_VOL) 2. Page 1 Command Modification 0xB3(Removed, VGH voltage setting by times, merge in 0xB9) 0xB5(Change to VGL_REG cmd, VGL voltage setting by time, merge in 0xBA) 0xB6, 0xB7(Removed AVDD/AVEE 3.5X, 4X function, update default) 0xB8(update default) 0xBA(Removed LVGL, change to VGLX) 0xD1 to 0xD6(Gamma 2.2 to 10 bits control) 0xE9 to 0x0xEB(Gamma1.0, 1.8, 2.5 to 10 bits control) 0xED(move B5xxh, BDxxh~BFxxh of page 0 to MTP_EN2[3]) 0xEF(move B5xxh, BDxxh~BFxxh of page 0 to MTP_STUS2[3]) 3. Pad chapter update 4. Timing Example update 5. Auto Sequence update 6. External component. C32 update	Kevin	SW	Dennis	2010/05/12

0.03	1. Page 0 Command Modification Page0/1 switch function modified 0xB1 (RGBBP removed) 0xB4 (vivid color type selection) 0xB9 (PTVCM removed, PT[1:0] to PTD[1:0]: description update) 0xD0, 0xD1,0xD6~0xD8,0xDF,0xE002,0xEC (KBBC function removed) 0xD2 (CMCT, DD_C removed, KBBC related bits) 0xD3~0xD5 (description update) 0xD9 (removed) 0xB5 (resolution typo) 0xB6~0xBB,0xBD (update Default Value) 0xBD,0xBE,0xBF (description update) 0xDD (update description) 0xE1,0xEA,0xEB (graph update) 2. Page 1 Command Modification 0xE9~0xEB,0xED01,0xC904,0xC905 (removed) 0xB6 (AVDD to 1.66X, default value update) 0xB7,0xB8,0xBB,0xEE,0xEF,0xD0~0xD6 (update Default Value) 0xBE,0xC6,0xED,0xEF (update description) 3. Maximum resistance (I2C_SA[1] to RGBBP) 4. DC/DC converter circuit update (add PFM circuit) 5. Component list update (add PFM components list) 6. Pad information update 7. Timing examples update 8. Add Serial interface of 4-pin SPI (8-bit) and 3-pin SPI (9-bit)	Henry	SW	Dennis	2010/07/30
0.04	1. Modify typo on page 134. 2. Modify the chip thickness from 250um to 200um on page 139. 3. Update Timing Examples 4. Add a new section 5.3 Mapping Table of Gate Control Signals on page 161.	Henry	SW	Dennis	2010/08/06
0.05	Page 0: Update Table 1.2.1 B0XXh: update restriction for vertical porch of RGB interface B5XXh: add restriction and remove 480RGBx360 B600h: add Note for SDT[5:0]=00h B901h: remove control bit PNG D0XXh: update description and remove control bit PWM_ENH_OE Update default: B800h, B9XXh Page 1: B9XXh: remove description in setting table of BTHA/B/C BAXXh: remove description in setting table of BTLA/B/C EDXXh: update MTP_EN1[4] as in-house MTP EFXXh: update MTP_STUS2[3] as in-house MTP Update default: B3XXh, B6XXh, B7XXh, B8XXh, B9XXh, BAXXh Others: Section 6.6: add Microprocessor Interface Mark “Page 0” and “Page 1” in each command Section 5.1: correct alignment mark coordinate	Henry	SW	Dennis	2010/10/18
0.06	1. Add the description of RDX pin on page 162.	Henry	SW	Dennis	2011/01/05

0.07	1. Add the resolution of 480RGBx360 in B500h.	Henry	SW	Dennis	2011/02/25

1 COMMAND DESCRIPTIONS

1.1 Manufacture Command Set Selection

Table 1.1.1 Manufacture Command Set

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
MAUCCTR	Dir	W	F0h	F000h	00h	0	1	0	1	0	1	0	1	Manufacture command enable
				F001h	00h	1	0	1	0	1	0	1	0	
				F002h	00h	0	1	0	1	0	0	1	0	
				F003h	00h	-	-	-	-	MAUC	-	-	-	
				F004h	00h	-	-	-	-	-	-	-	PAGE	

NOTE:

1. The following description indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line

2. The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit SPI and 4-wire 8-bit SPI.

MAUCCTR: Manufacture Command Set Control (F000h~F003h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MAUCCTR	W	F0h	F000h	00h	0	1	0	1	0	1	0	1
			F001h	00h	1	0	1	0	1	0	1	0
			F002h	00h	0	1	0	1	0	0	1	0
			F003h	00h	-	-	-	-	MAUC	-	-	-
			F004h	00h	-	-	-	-	-	-	-	PAGE

NOTE: "-" Don't care

Description

This command is used to enable/disable the Manufacture Command Set and select the page 0 or page 1 of Manufacture Command Set. Address B0xxh~D9xxh, DDxxh~DFxxh and E0xxh~EFxxh for each page.

Bit	Description	Value
MAUC	Manufacture Command Set enable/disable	"0": Manufacture Command Set disable "1": Manufacture Command Set enable
PAGE	Manufacture Command Set selection	"0": Page 0 "1": Page 1

Note: This command is always enable even Manufacture Command Set is disable.

Restriction

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Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	F000h	F001h	F002h	F003h (MAUC)	F004h (PAGE)
Power On Sequence	55h	AAh	52h	00h	00h
S/W Reset	55h	AAh	52h	00h	00h
H/W Reset	55h	AAh	52h	00h	00h

1.2 Manufacture Command Set for Page 0

Table 1.2.1 Manufacture Command Set – Page 0

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RGBCTR	DVS	R/W	B0h	B000h	00h	CMRC	VSDL	HSDL	DEDL	PCKP	DEP	HSP	VSP	Set delay, polarity and porch for RGB I/F
				B001h	00h	VBP[7:0]								
				B002h	00h	VFP[7:0]								
				B003h	00h	HBP[7:0]								
				B004h	00h	HFP[7:0]								
DOPCTR	Dir	R/W	B1h	B100h	00h	RAMKP	DSITE	DSIG	DSIM	DIS_EoTP_HS	N565	ERR[1:0]		Display optional control
	DVS			B101h	00h	-	-	-	TE_PWR_SEL	CRGB	CTB	CRL	-	
DPCKRGB	DVS	R/W	B3h	B300h	00h	-	-	-	-	-	-	-	ICM	Display clock selection in RGB I/F
VIVIDCTR	DVS	R/W	B4h	B400h	00h	-	-	-	VCEN	-	-	~~VCSEL[1:0]~~		Control for vivid color function
DPRSLCTR	DVS	R/W	B5h	B500h	00h	CGM[7:0]								Display resolution control
SDHDTCTR	DVS	R/W	B6h	B600h	00h	-	-	SDT[5:0]						Set source output data hold time
GSEQCTR	DVS	R/W	B7h	B700h	00h	GREQ_ST[3:0]				GFEQ_ST[3:0]				EQ control function for gate signals
				B701h	00h	GREQ_CK[3:0]				GFEQ_CK[3:0]				
SDEQCTR	DVS	R/W	B8h	B800h	00h	-	-	-	-	-	-	-	EQMOD	Source control for EQ function
				B801h	00h	-	-	-	-	-	EQS1[3:0]			
				B802h	00h	-	-	-	-	-	EQS2[3:0]			
				B803h	00h	-	-	-	-	-	EQS3[3:0]			
SDNDACTR	DVS	R/W	B9h	B900h	00h	-	-	-	-	ISCI[3:0]				Source/VCOM control in non-display area of partial mode
				B901h	00h	-	GOAX	PTD[1:0]		-	-	PT[1:0]		
SDVPCTR	DVS	R/W	BAh	BA00h	00h	-	-	-	-	-	PRG	PR[1:0]		Source/VCOM/Gate control in V-porch
SGOPCTR	DVS	R/W	BBh	BB00h	00h	ISOPA[3:0]				IGOPA[3:0]				Set bias current of GOP and SOP
				BB01h	00h	-	-	-	-	IGOPB[3:0]				
				BB02h	00h	ISOPC[3:0]				IGOPC[3:0]				
INVCTR	DVS	R/W	BCh	BC00h	00h	-	-	-	-	-	NLA[2:0]			Inversion control
				BC01h	00h	-	-	-	-	-	NLB[2:0]			
				BC02h	00h	-	-	-	-	-	NLC[2:0]			
DPFRCTR1	DVS	R/W	BDh	BD00h	00h	-	-	-	-	-	-	T1A[9:8]		Display timing control for normal / idle off mode in non-RGB I/F
				BD01h	00h	T1A[7:0]								
				BD02h	00h	VBPDA[7:0]								
				BD03h	00h	VFPDA[7:0]								
				BD04h	00h	-	-	-	-	-	-	PSELA[1:0]		
DPFRCTR2	DVS	R/W	BEh	BE00h	00h	-	-	-	-	-	-	T1B[9:8]		Display timing control for idle on mode in non-RGB I/F
				BE01h	00h	T1B[7:0]								
				BE02h	00h	VBPDB[7:0]								
				BE03h	00h	VFPDB[7:0]								
				BE04h	00h	-	-	-	-	-	-	PSELB[1:0]		
DPFRCTR3	DVS	R.W	BFh	BF00h	00h	--	--	--	--	-	-	T1C[9:8]		Display timing control for partial / idle off mode in non-RGB I/F
				BF01h	00h	T1C[7:0]								
				BF02h	00h	VBPDC[7:0]								
				BF03h	00h	VFPDC[7:0]								
				BF04h	00h	-	-	-	-	-	-	PSELC[1:0]		
DPTMCTR12	DVS	R/W	CCh	CC00h	00h	-	-	-	LVGL SEL_H	-	-	FHN	LR_H	Timing control VGSW = 1100
				CC01h	00h	CLW_H[7:0]								
				CC02h	00h	FTI_H[7:0]								

Table 1.2.1 Manufacture Command Set – Page 0 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
LEDCTRDP	Dir	R/W	D0h	D000h	00h	-	-	LEDONR	LEDONPOL	LEDPWM_OEB	CLED_VOL	~~PWM_ENH_OE~~	LEDPWPOL	Control for LEDON/LEDPWM pins
DIMCTR	DVS	R/W	D2h	D200h	00h	-	-	-	-	SEL_IN	SEL_DE	-	-	Dimming control for CABC and LABC
DIMCTRDP1	DVS	R/W	D3h	D300h	00h	DM_IN[3:0]				DM_DE[3:0]				Time per step for display brightness by LABC (fixed-time & fixed- slope)
DIMCTRDP2	DVS	R/W	D4h	D400h	00h	-	-	-	-	-	DMSTP_L[2:0]			Total steps for display brightness by LABC (fixed-time)
DIMCTRDP3	DVS	R/W	D5h	D500h	00h	STEP_IN[3:0]				STEP_DE[3:0]				Brightness change per step for display brightness by LABC (fixed-slope)
DIMCTRCB2	DVS	R/W	DDh	DD00h	00h	-	DIM_STEP_MOV[2:0]			-	DIM_STEP_STILL[2:0]			Total steps for display brightness by CABC (fixed-time)
PWMOFFDP	Dir	R/W	DEh	DE00h	00h	-	-	-	PWM_DUTY_OFFSET[4:0]					Compensate effective PWM duty for LEDPWM
PWMFRCTR	Dir	R/W	E0h	E000h	00h	-	-	-	-	-	-	-	PWMF	PWM frequency adjustment for LEDPWM
				E001h	00h	PWMDIV [7:0]								
FCBRTCB	Dir	R/W	E1h	E100h	00h	-	-	-	-	-	-	-	FORCE_CABC_PWM	Force display brightness for CABC
				E101h	00h	FORCE_CABC_DUTY[7:0]								
BRTCBUI	Dir	R/W	E2h	E200h	00h	CABC_UI_PWM0[7:0]								Display brightness setting corresponding to different gamma algorithm in CABC UI-mode
				E201h	00h	CABC_UI_PWM1[7:0]								
				E202h	00h	CABC_UI_PWM2[7:0]								
				E203h	00h	CABC_UI_PWM3[7:0]								
BRTCBSTL	Dir	R/W	E3h	E300h	00h	CABC_PWM0[7:0]								Display brightness setting corresponding to different gamma algorithm in CABC Still-mode
				E301h	00h	CABC_PWM1[7:0]								
				E302h	00h	CABC_PWM2[7:0]								
				E303h	00h	CABC_PWM3[7:0]								
				E304h	00h	CABC_PWM4[7:0]								
				E305h	00h	CABC_PWM5[7:0]								
				E306h	00h	CABC_PWM6[7:0]								
				E307h	00h	CABC_PWM7[7:0]								
				E308h	00h	CABC_PWM8[7:0]								
				E309h	00h	CABC_PWM9[7:0]								
BRTCBMOV	Dir	R/W	E4h	E400h	00h	CABC_MOV_PWM0[7:0]								Display brightness setting corresponding to different gamma algorithm in CABC Moving-mode
				E401h	00h	CABC_MOV_PWM1[7:0]								
				E402h	00h	CABC_MOV_PWM2[7:0]								
				E403h	00h	CABC_MOV_PWM3[7:0]								
				E404h	00h	CABC_MOV_PWM4[7:0]								
				E405h	00h	CABC_MOV_PWM5[7:0]								
				E406h	00h	CABC_MOV_PWM6[7:0]								
				E407h	00h	CABC_MOV_PWM7[7:0]								
				E408h	00h	CABC_MOV_PWM8[7:0]								
				E409h	00h	CABC_MOV_PWM9[7:0]								

Table 1.2.1 Manufacture Command Set – Page 0 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
AMOVCTR	Dir	R/W	E5h	E500h	00h	-	MOVDET[6:0]							Automatic moving mode detection control
				E501h	00h	-	-	-	MOVSC[4:0]					
FHYSTCTR	Dir	R/W	E6h	E600h	00h	SET_HYST	-	-	-	HYST_OUT_VAL[3:0]				Final hysteresis result control
HYSTCTR	Dir	R/W	E7h	E700h	00h	HYST_EN	-	-	-	HYST_WR[3:0]				Internal hysteresis control
FLTRCTR	Dir	R/W	E8h	E800h	00h	MRF_BYS	-	-	-	FKP[3:0]				Median filter and flicker filter control
WRALSV	Dir	R/W	E9h	E900h	00	LS[7:0]								Write given ambient light information into LABC circuit
				E901h	00h	LS[15:8]								
				E902h	00h	-	-	-	-	-	-	-	ALS_W	
RDBRTDPL	Dir	R	EAh	EA00h	00h	RDPWM_L[7:0]								Read display brightness value from LABC
RDBRTDPC	Dir	R	EBh	EB00h	00h	RDPWM[7:0]								Read display brightness value from CABC
RDHYST	Dir	R	EDh	ED00h	00h	-	-	-	-	RD_HYST_OUT[3:0]				Read output hysteresis result of internal hysteresis block
RDGMA	Dir	R	EEh	EE00h	00h	RD_GMA_SET[7:0]								Read gamma curve for current display
RDALSV	Dir	R	EFh	EF00h	00	ALSV[7:0]								Read the ambient light information
				EF01h	00h	ALSV[15:8]								

NOTE:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line

2. The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit SPI and 4-wire 8-bit SPI.

RGBCTR: RGB Interface Signals Control (Page 0, B000h~B004h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RGBCTR	R/W	B0h	B000h	00h	CRCM	VSDL	HSDL	DEDL	PCKP	DEP	HSP	VSP
			B001h	00h	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
			B002h	00h	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0
			B003h	00h	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
			B004h	00h	HFP7	HFP6	HFP5	HFP4	HFP3	HFP2	HFP1	HFP0

NOTE: "-" Don't care

Description

This command is used to define the operation status and vertical / horizontal porch of RGB interface. The setting becomes effective as soon as the command is received.

Bit	Description	Value
CRCM	Select the RGB mode1/mode 2	"0" = RGB mode 1
		"1" = RGB mode 2
VSDL	VS Delay Setting	"0" = No delay
		"1" = Delay 0.5 PCLK
HSDL	HS Delay Setting	"0" = No delay
		"1" = Delay 0.5 PCLK
DEDL	DE Delay Setting	"0" = No delay
		"1" = Delay 0.5 PCLK
PCKP	PCLK Fetch Polarity	"0" = Data latched at the rising edge of PCLK
		"1" = Data latched at the falling edge of PCLK
DEP	DE Enable Polarity	"0" = High enable for RGB interface
		"1" = Low enable for RGB interface
HSP	H-Sync Pulse Level	"0" = Low pulse level sync clock
		"1" = High pulse level sync clock
VSP	V-Sync Pulse Level	"0" = Low pulse level sync clock
		"1" = High pulse level sync clock
VBP[7:0]	V-Sync Back Porch	"05h" to "FFh" = 5 to 255 H-Sync clocks
VFP[7:0]	V-Sync Front Porch	"02h" to "FFh" = 2 to 255 H-Sync clocks
HBP[7:0]	H-Sync Back Porch	"05h" to "FFh" = 5 to 255 PCLK clocks
HFP[7:0]	H-Sync Front Porch	"02h" to "FFh" = 2 to 255 PCLK clocks

The registers VBP[7:0], VFP[7:0], HBP[7:0] and HFP[7:0] for vertical and horizontal porch control are used in RGB interface mode 2 only. The setting value "00h" is invalid for all of these four registers.

RGB IF Mode	PCLK	DE	D[23:0]	VS	HS	VBP[7:0], VFP[7:0], HBP[7:0], HFP[7:0]
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Restriction

VFP[5:0] ≥ "02h", VBP[5:0] ≥ "05h" and VFP[7:0]+VBP[7:0] > VBPDA/B/C[7:0]
HFP[5:0] ≥ "02h", HBP[5:0] ≥ "05h"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	B000h	B001h (VBP)	B002h (VFP)	B003h (HBP)	B004h (HFP)
Power On Sequence	00h	05h	02h	05h	02h
S/W Reset	00h	05h	02h	05h	02h
H/W Reset	00h	05h	02h	05h	02h

DOPCTR: Display Option Control (Page 0, B100h~B101h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DOPCTR	R/W	B1h	B100h	00h	RAMKP	DSITE	DSIG	DSIM	DIS_EoTP_HS	N565	ERR1	ERR0
			B101h	00h	-	-	-	TE_PWR_SEL	CRGB	CTB	CRL	-

NOTE: "-" Don't care

Description

This command is used to do some optional control for display and application.

Bit	Description	Value
RAMKP	Frame Memory keep/loss in Sleep-in mode	"0": Contents loss in sleep-in "1": Contents keep in sleep-in
DSITE	TE line enable/disable	"0": TE line is disabled "1": TE line is enabled
DSIG	Generic read/write data type enable/disable for MIPI DSI	"0": Generic read/write disable "1": Generic read/write enable
DSIM	Video mode data type enable/disable for MIPI DSI	"0": Video mode data type disable "1": Video mode data type enable
DIS_EoTP_HS	"DSI Protocol Violation" error reporting enable/disable control	"0": enable, reporting when error "1": disable, not reporting when error
N565	16-bit/pixel format (MSB to LSB) selection in MIPI command mode	"0": R[4:0]+G[5:3] & G[2:0]+B[4:0] "1": G[2 :0]+R[4 :0] & B[4 :0]+G[5 :3]
ERR[1:0]	ERR pin output signal setting	"00": Disable, ERR pin output low "01": ERR pin output CRC error only "10": ERR pin output ECC error only "11": ERR pin output CRC and ECC error
TE_PWR_SEL	TE output voltage level selection (only valid when DSTB_SEL=0 or DSTB_SEL=1, VSEL=High and VDDI=1.65~3.3V)	TE_PWR_SEL: 0 → TE Output Voltage Level: VSSI to VDDI TE_PWR_SEL: 1 → TE Output Voltage Level: VSSI to DIOPWR
CRGB	RGB-BGR Order selection. This bit is XOR operation with bit RGB of 3600h	CRGB: 0, RGB: 0 → Order: RGB, Gamma: Normal CRGB: 0, RGB: 1 → Order: BGR, Gamma: RB swap CRGB: 1, RGB: 0 → Order: BGR, Gamma: RB swap CRGB: 1, RGB: 1 → Order: RGB, Gamma: Normal
CTB	Vertical scanning direction selection for gate control signals. This bit is XOR operation with bit ML of 3600h.	CTB: 0, ML: 0 → Direction: Forward (top→bottom) CTB: 0, ML: 1 → Direction: Reverse(Bottom→top) CTB: 1, ML: 0 → Direction: Reverse (Bottom→top) CTB: 1, ML: 1 → Direction: Forward (top→bottom)

Description

Bit	Description	Value
CRL	Source driver data shift direction selection (see section 8.2). This bit is XOR operation with bit RSMX of 3600h command	

CRL	RSMX	Direction
0	0	S1 → S1440
0	1	S1440 → S1
1	0	S1440 → S1
1	1	S1 → S1440

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	B100h	B101h
Power On Sequence	4Ch	00h
S/W Reset	4Ch	00h
H/W Reset	4Ch	00h

DPCKRGB: Display Clock in RGB Interface (Page 0, B300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPCKRGB	Write	X	B300h	00h	0	0	0	0	0	0	0	ICM

NOTE: "-" Don't care

Description

This command is used to select SRAM data input path and display clock in RGB interface.

ICM	Data Write to SRAM		SRAM Data Read to Display
	SRAM Write Clock	SRAM Data Input Path	Internal Display Clock
0	PCLK	D[23:0]	VS, HS and PCLK
1	SCL	SDI	Internal Oscillator

Note: This command is active in RGB interface only.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ICM = "0"
S/W Reset	ICM = "0"
H/W Reset	ICM = "0"

VIVIDCTR: Vivid Color Function Control (Page 0, B400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
VIVIDCTR	R/W	B4h	B400h	00h	-	-	-	VCEN	-	-	-	-

NOTE: "-" Don't care

Description

This command is used to control vivid color function.

Bit	Description	Value
VCEN	Enable control for vivid color function	"0": Disable
		"1": Enable

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	B400h
S/W Reset	00h
H/W Reset	00h

DPRSLCTR: Display Resolution Control (Page 0, B500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPRSLCTR	R/W	B5h	B500h	00h	CGM7	CGM6	CGM5	CGM4	CGM3	CGM2	CGM1	CGM0

NOTE: "-" Don't care

Description

This command is used to control the display resolution.

CGM[7:0]: display scan line setting.

CGM[7:0]	Display Resolution
00h	480RGB x 640
01h	480RGB x 642
02h	480RGB x 644
:	: (2 lines/Step)
28h	480RGB x 720
:	: (2 lines/Step)
50h	480RGB x 800
:	: (2 lines/Step)
6Bh	480RGB x 854
:	: (2 lines/Step)
70h	480RGB x 864
:	: (2 lines/Step)
BEh	480RGB x 1020
BFh	480RGB x 1022
C0h	480RGB x 1024
FEh	480RGB x 360
Others	reserved

Note: The scan line settings, which larger than 864 lines, are used for RGB interface by pass mode only (RGBBP=VDDI) and the scan lines will be fixed at 864 lines when RGBBP is connected to VSSI.

Restriction

This command should be excuted during sleep-in mode

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	B500h
Power On Sequence	50h
S/W Reset	50h
H/W Reset	50h

SDHDTCTR: Source Output Data Hold Time Control (Page 0, B600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SDHDTCTR	R/W	B6h	B600h	00h	-	-	SDT5	SDT4	SDT3	SDT2	SDT1	SDT0

NOTE: "-" Don't care

Description

This command is used to control the source output data hold time.

SDT[5:0]: set source output data hold time.

SDT[5:0]	No. of Clock	Data Hold Time
00h	0	0.0µs
01h	10	0.5µs
02h	20	1.0µs
:	:	: (0.5µs/Step)
05h	50	2.5µs
:	:	: (0.5µs/Step)
3Dh	610	30.5µs
3Eh	620	31.0µs
3Fh	630	31.5µs

Note: Set EQMOD0=1 (command B800h, select source EQ mode 2) if SDT[5:0]=00h is used

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	B600h (SDT)
Power On Sequence	05h
S/W Reset	05h
H/W Reset	05h

GSEQCTR: EQ Control Function for Gate Signals (Page 0, B700h~B701h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GSEQCTR	R/W	B7h	B700h	00h	GREQ_ST3	GREQ_ST2	GREQ_ST1	GREQ_ST0	GFEQ_ST3	GFEQ_ST2	GFEQ_ST1	GFEQ_ST0
			B701h	00h	GREQ_CK3	GREQ_CK2	GREQ_CK1	GREQ_CK0	GFEQ_CK3	GFEQ_CK2	GFEQ_CK1	GFEQ_CK0

NOTE: "-" Don't care

Description

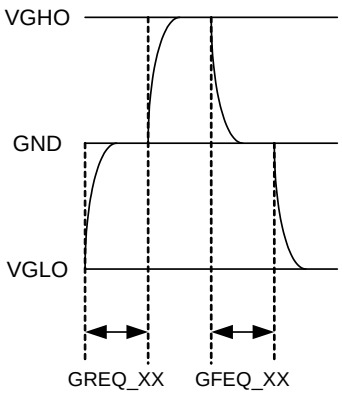
This command is used to control the EQ function for gate signals.

GREQ_XX[3:0]: time setting of EQ step for rising edge.

GREQ_ST[3:0]	No. of Clock	EQ for Rising Edge	GREQ_CK[3:0]	No. of Clock	EQ for Rising Edge
0h	0	0.0µs	0h	0	0.0µs
1h	10	0.5µs	1h	10	0.5µs
2h	20	1.0µs	2h	20	1.0µs
:	:	: (0.5µs/Step)	:	:	: (0.5µs/Step)
7h	70	3.5µs	7h	70	3.5µs
:	:	: (0.5µs/Step)	:	:	: (0.5µs/Step)
Dh	130	6.5µs	Dh	130	6.5µs
Eh	140	7.0µs	Eh	140	7.0µs
Fh	150	7.5µs	Fh	150	7.5µs

GFEQ_XX[3:0]: time setting of EQ step for falling edge.

GFEQ_ST[3:0]	No. of Clock	EQ for Falling Edge	GFEQ_CK[3:0]	No. of Clock	EQ for Falling Edge
0h	0	0.0µs	0h	0	0.0µs
1h	10	0.5µs	1h	10	0.5µs
2h	20	1.0µs	2h	20	1.0µs
:	:	: (0.5µs/Step)	:	:	: (0.5µs/Step)
7h	70	3.5µs	7h	70	3.5µs
:	:	: (0.5µs/Step)	:	:	: (0.5µs/Step)
Dh	130	6.5µs	Dh	130	6.5µs
Eh	140	7.0µs	Eh	140	7.0µs
Fh	150	7.5µs	Fh	150	7.5µs



<table>
<tr><td>Description</td><td>The GREQ_XX and GFEQ_XX are used to control EQ function for different gate signals as below.
<table>
<tr><td>GREQ_ST[3:0], GFEQ_ST[3:0]</td><td>GREQ_CK[3:0], GFEQ_CK[3:0]</td></tr>
<tr><td>-</td><td>STP_O/E, CK_O/E, CKB_O/E</td></tr>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td>
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<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>B700h (GREQ_ST, GFEQ_ST)</th><th>B701h (GREQ_CK, GFEQ_CK)</th></tr>
<tr><td>Power On Sequence</td><td>77h</td><td>77h</td></tr>
<tr><td>S/W Reset</td><td>77h</td><td>77h</td></tr>
<tr><td>H/W Reset</td><td>77h</td><td>77h</td></tr>
</table></td></tr>
</table>

SDEQCTR: EQ Control Function for Source Driver (Page 0, B800h~B803h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SDEQCTR	R/W	B8h	B800h	00h	-	-	-	-	-	-	-	EQ MOD
			B801h	00h	-	-	-	-	EQS13	EQS12	EQS11	EQS10
			B802h	00h	-	-	-	-	EQS23	EQS22	EQS21	EQS20
			B803h	00h	-	-	-	-	EQS33	EQS32	EQS31	EQS30

NOTE: "-" Don't care

Description

This command is used to control the EQ function for source driver.

EQMOD: EQ mode 1/mode 2 selection

EQMOD	EQ Mode
0	EQ mode 1
1	EQ mode 2

EQS1[3:0]: time setting for EQ step 1

EQS1[3:0]	No. of Clock	Time for EQ Step 1
0h	0	0.0µs
1h	10	0.5µs
:	:	: (0.5µs/Step)
7h	70	3.5µs
:	:	: (0.5µs/Step)
Eh	140	7.0µs
Fh	150	7.5µs

EQS2[3:0]: time setting for EQ step 2

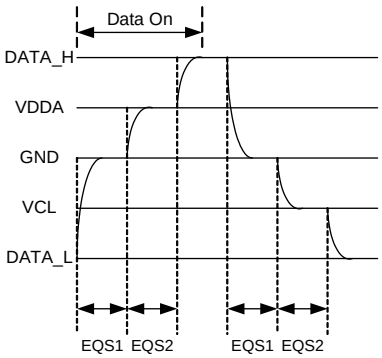
EQS2[3:0]	No. of Clock	Time for EQ Step 2
0h	0	0.0µs
1h	10	0.5µs
:	:	: (0.5µs/Step)
7h	70	3.5µs
:	:	: (0.5µs/Step)
Eh	140	7.0µs
Fh	150	7.5µs

EQS3[3:0]: time setting for EQ step 3

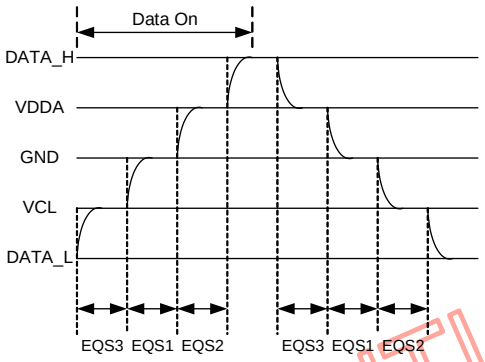
EQS3[3:0]	No. of Clock	Time for EQ Step 3
0h	0	0.0µs
1h	10	0.5µs
:	:	: (0.5µs/Step)
7h	70	3.5µs
:	:	: (0.5µs/Step)
Eh	140	7.0µs
Fh	150	7.5µs

Description

EQ Mode 1



EQ Mode 2



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	B800h	B801h (EQS1)	B802h (EQS2)	B803h (EQS3)
Power On Sequence	01h	07h	07h	07h
S/W Reset	01h	07h	07h	07h
H/W Reset	01h	07h	07h	07h

SDNDACTR: Source Control in Non-Display Area of Partial Display (Page 0, B900h~B901h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SDNDACTR	R/W	B9h	B900h	00h	-	-	-	-	ISCI3	ISCI2	ISCI1	ISCI0
			B901h	00h	-	GOAX	PTD1	PTD0	-	-	PT1	PT0

NOTE: "-" Don't care

Description

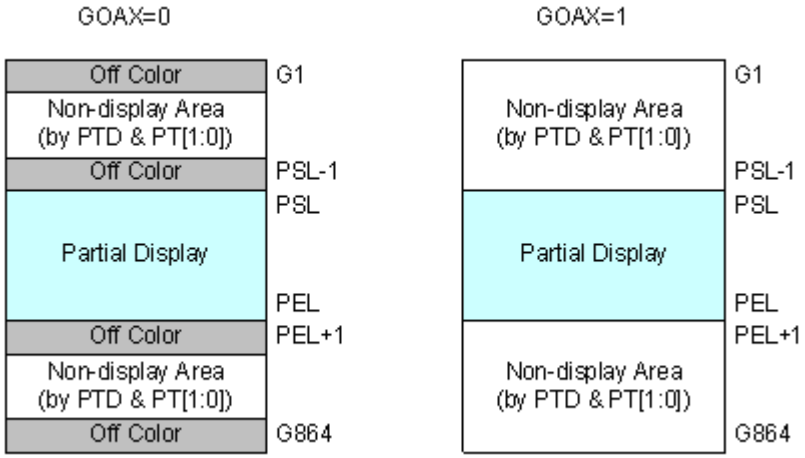
This command is used to control the output status of source driver, VCOM and the refresh rate in non-display area for partial display.

ISCI[3:0]: the refresh rate for non-display area in Partial Mode.

ISCI[3:0]	Refresh Rate for Non-display Area
0h	Full scan
1h	3 frames
2h	5 frames
3h	7 frames
:	: (2 frames/Step)
Eh	29 frames
Fh	31 frames

GOAX: the source output status in the 1st line and the last line of non-display area for partial display.

GOAX	Source Output Status in the Non-display Area
0	Off color
1	By PTD and PT[1:0] setting



Description

PTD[1:0]: the source output status in non-display area of partial display when refresh frame.

PTD[1:0]	Source Output Status in the Non-display Area when Refresh
00	Off color
01	Anti-Off color
10	AVSS
11	AVDD

PT[1:0]: the source output status in non-display area of partial display when non-refresh frames.

PT[1:0]	Source Output Status in the Non-display Area when Non-refresh
00	Off color
01	Anti-Off color
10	AVSS
11	Hi-Z

Example: When ISCI[3:0] is set to "01h", the refresh rate for non-display area is 3 frames and the function of PTD and PT[1:0] for non-display area are shown below.

Frame No.	1st Frame	2nd Frame	3rd Frame	4th Frame	·····
	Refresh	Non-Refresh	Non-Refresh	Refresh	·····
Source Data	Off or Anti-Off by PTD setting	by PT[1:0] setting	by PT[1:0] setting	Off or Anti-Off by PTD setting	·····

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	B900h (ISCI)	B901h
Power On Sequence	00h	40h
S/W Reset	00h	40h
H/W Reset	00h	40h

SDVPCTR: Source Control in Vertical Porch Time (Page 0, BA00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SDVPCTR	R/W	BAh	BA00h	00h	-	-	-	-	-	PRG	PR1	PR0

NOTE: "-" Don't care

Description

This command is used to control the output status of source driver, gate signals and VCOM in vertical porch time.

PRG: the output status for gate signals in vertical porch time.

PRG	Gate Signals Status
0	Normal operation
1	VGLO

Note: Vertical Scan Lines+Vertical Porch Lines = multiple of 4 if PRG is set to "0".
(refer to command BDXXh, BEXXh and BFXXh).

PR[1:0]: the output status for source driver in vertical porch time.

PR[1:0]	Source Output Status
00	AVDD
01	Off color
10	AVSS
11	Hi-Z

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BA00h
Power On Sequence	05h
S/W Reset	05h
H/W Reset	05h

SGOPCTR: Source Driver Control (Page 0, BB00h~BB02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SGOPCTR	R/W	BBh	BB00h	00h	ISOPA3	ISOPA2	ISOPA1	ISOPA0	IGOPA3	IGOPA2	IGOPA1	IGOPA0
			BB01h	00h	-	-	-	-	IGOPB3	IGOPB2	IGOPB1	IGOPB0
			BB02h	00h	ISOPC3	ISOPC2	ISOPC1	ISOPC0	IGOPC3	IGOPC2	IGOPC1	IGOPC0

NOTE: "-" Don't care

Description

This command is used to control the bias current of GOP and SOP in different display mode.

ISOPA[3:0]: the bias current for source OP in normal / idle off mode.
ISOPC[3:0]: the bias current for source OP in partial / idle off mode.

ISOPA[3:0] ISOPC[3:0]	Bias Current of Source OP	ISOPA[3:0] ISOPC[3:0]	Bias Current of Source OP
0h	Minimum	8h	Medium Low
1h	Minimum High	9h	Medium
2h	Small Low	Ah	Medium High
3h	Small	Bh	Large Low
4h	Small High	Ch	Large
5h	Small Medium Low	Dh	Large High
6h	Small Medium	Eh	Maximum Low
7h	Small Medium High	Fh	Maximum

IGOPA[3:0]: the bias current for source OP in normal / idle off mode.
IGOPB[3:0]: the bias current for source OP in idle on mode.
IGOPC[3:0]: the bias current for source OP in partial / idle off mode.

IGOPA[3:0] IGOPB[3:0] IGOPC[3:0]	Bias Current of Gamma OP	IGOPA[3:0] IGOPB[3:0] IGOPC[3:0]	Bias Current of Source OP
0h	Minimum	8h	Medium Low
1h	Small	9h	Medium
2h	Medium Low	Ah	Medium High
3h	Medium	Bh	Large Low
4h	Medium High	Ch	Large
5h	Large	Dh	Large High
6h	Large High	Eh	Maximum Low
7h	Maximum	Fh	Maximum

<table>
<tr><td>Restriction</td><td>-</td></tr>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>BB00h</th><th>BB01h</th><th>BB02h</th></tr>
<tr><td>Power On Sequence</td><td>22h</td><td>02h</td><td>22h</td></tr>
<tr><td>S/W Reset</td><td>22h</td><td>02h</td><td>22h</td></tr>
<tr><td>H/W Reset</td><td>22h</td><td>02h</td><td>22h</td></tr>
</table>
</td></tr>
</table>

INVCTR: Inversion Driving Control (Page 0, BC00h~BC02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVCTR	R/W	BCh	BC00h	00h	-	-	-	-	-	NLA2	NLA1	NLA0
			BC01h	00h	-	-	-	-	-	NLB2	NLB1	NLB0
			BC02h	00h	-	-	-	-	-	NLC2	NLC1	NLC0

NOTE: "-" Don't care

Description

This command is used to control the inversion mode for source driver.

NLA[2:0]: the inversion mode for source driver in normal / idle off mode.
NLB[2:0]: the inversion mode for source driver in idle on mode.
NLC[2:0]: the inversion mode for source driver in partial / idle off mode.

NLA[2:0], NLB[2:0], NLC[2:0]	Inversion Mode for Source Driver
000	Column inversion
001	1-dot inversion
010	2-dot inversion
011	3-dot inversion
100	4-dot inversion
101~111	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BC00h (NLA)	BC01h (NLB)	BC02h (NLC)
Power On Sequence	00h	00h	00h
S/W Reset	00h	00h	00h
H/W Reset	00h	00h	00h

DPFRCTR1: Display Timing Control in Normal / Idle Off Mode (Page 0, BD00h~BD04h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPFRCTR1	R/W	BDh	BD00h	00h	-	-	-	-	-	-	T1A9	T1A8
			BD01h	00h	T1A7	T1A6	T1A5	T1A4	T1A3	T1A2	T1A1	T1A0
			BD02h	00h	VBPDA 7	VBPDA 6	VBPDA 5	VBPDA 4	VBPDA 3	VBPDA 2	VBPDA 1	VBPDA 0
			BD03h	00h	VFPDA 7	VFPDA 6	VFPDA 5	VFPDA 4	VFPDA 3	VFPDA 2	VFPDA 1	VFPDA 0
			BD04h	00h	-	-	-	-	-	-	PSELA 1	PSELA 0

NOTE: "-" Don't care

Description

This command is used to set the display time of one scan line (Hsync), the vertical blanking porch line, and pixel clock frequency for display timing in normal / idle off mode.

T1A[9:0]: the display time of one scan line in normal / idle off mode.

T1A[9:0]	No. of Pixel Clock	Display Time for One Scan Line (Pixel Clock=20 MHz)
0d~256d	-	reserved
257d	258	12.90 µs
258d	259	12.95 µs
:	:	: (0.05 µs/Step)
388d	389	19.45 µs
:	:	: (0.05 µs/Step)
1022d	1023	51.15 µs
1023d	1024	51.20 µs

VBPDA[7:0]: the vertical back porch lines in normal / idle off mode.
VFPDA[7:0]: the vertical front porch lines in normal / idle off mode.

VBPDA[7:0]	No. of Vertical Porch Line	VFPDA[7:0]	No. of Vertical Porch Line
00h~01h	reserved	00h~01h	reserved
02h	2 lines	02h	2 lines
03h	3 lines	03h	3 lines
:	: (1 line/Step)	:	: (1 line/Step)
1Ch	28 lines	1Ch	28 lines
:	: (1 line/Step)	:	: (1 line/Step)
FEh	254 lines	FEh	254 lines
FFh	255 lines	FFh	255 lines

PSELA[1:0]: the pixel clock frequency selection in normal / idle off mode.

PSELA[1:0]	Divisor Condition
00h	1
01h	2
02h	4
03h	8

Description

The display frame frequency is decided by T1A[9:0] and this vertical porch lines as below.

$$\text{Frame Rate} = \frac{\frac{20\,\text{MHz}}{\text{PSELA}}}{\text{T1A} \times (\text{VBPDA} + \text{VFPDA} + \text{Vertical Scanning Lines})}$$

The setting values of T1A[9:0, VBPDA[7:0] and VFPDA[7:0] to keep the width of vertical porch>1ms for different display resolution are shown as below.

CGM[7:0]	Display Resolution	Default Value		Default Value (VBPDA+VFPDA)			Frame rate (Hz)
		T1A[9:0]	µs	VBPDA[7:0]	VFPDA[7:0]	ms	
FEh	480x360	0363h (867d)	43.40	0Ch (12d)	0Ch (12d)	1.042	60.00
00h	480x640	01E3h (483d)	24.20	18h (24d)	18h (24d)	1.162	60.06
28h	480x720	01B1h (433d)	21.70	18h (24d)	18h (24d)	1.042	60.00
50h	480x800	0184h (388d)	19.45	1Ch (28d)	1Ch (28d)	1.089	60.06
6Bh	480x854	016Ch (364d)	18.25	1Dh (29d)	1Dh (29d)	1.058	60.08
70h	480x864	0166h (358d)	17.95	20h (32d)	20h (32d)	1.149	60.03

Restriction

T1A[9:0] ≥ 101h (257d)
VBPDA[7:0] ≥ 6, VFPDA[7:0] ≥ 6
VBPDA[7:0]+VFPDA[7:0]+Vertical Scan Lines = multiple of 4 if PRG="0"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	BD00h, BD01h (T1A)	BD02h (VBPDA)	BD03h (VFPDA)	BD04h (PSELA)
Power On Sequence	01h, 84h	1Ch	1Ch	00h
S/W Reset	01h, 84h	1Ch	1Ch	00h
H/W Reset	01h, 84h	1Ch	1Ch	00h

DPFRCTR2: Display Timing Control in Idle On Mode (Page 0, BE00h~BE04h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPFRCTR2	R/W	BEh	BE00h	00h	-	-	-	-	-	-	T1B9	T1B8
			BE01h	00h	T1B7	T1B6	T1B5	T1B4	T1B3	T1B2	T1B1	T1B0
			BE02h	00h	VBPDB7	VBPDB6	VBPDB5	VBPDB4	VBPDB3	VBPDB2	VBPDB1	VBPDB0
			BE03h	00h	VFPDB7	VFPDB6	VFPDB5	VFPDB4	VFPDB3	VFPDB2	VFPDB1	VFPDB0
			BE04h	00h	-	-	-	-	-	-	PSELB1	PSELB0

NOTE: "-" Don't care

Description

This command is used to set the display time of one scan line (Hsync), the vertical blanking porch line, and pixel clock frequency for display timing in idle on mode.

T1B[9:0]: the display time of one scan line in idle on mode.

T1B[9:0]	No. of Pixel Clock	Display Time for One Scan Line (Pixel Clock=20 MHz)
0d~256d	-	reserved
257d	258	12.90 µs
258d	259	12.95 µs
:	:	: (0.05 µs/Step)
388d	389	19.45 µs
:	:	: (0.05 µs/Step)
1022d	1023	51.15 µs
1023d	1024	51.20 µs

VBPDB[7:0]: the vertical back porch lines in idle on mode.
VFPDB[7:0]: the vertical front porch lines in idle on mode.

VBPDB[7:0]	No. of Vertical Porch Line	VFPDB[7:0]	No. of Vertical Porch Line
00h~01h	reserved	00h~01h	reserved
02h	2 lines	02h	2 lines
03h	3 lines	03h	3 lines
:	: (1 line/Step)	:	: (1 line/Step)
1Ch	28 lines	1Ch	28 lines
:	: (1 line/Step)	:	: (1 line/Step)
FEh	254 lines	FEh	254 lines
FFh	255 lines	FFh	255 lines

PSELB[1:0]: the pixel clock frequency selection in idle on mode.

PSELB[1:0]	Divisor Condition
00h	1
01h	2
02h	4
03h	8

<table>
<tr><td>Description</td><td>The display frame frequency is decided by T1B[9:0] and this vertical porch lines as below.
$$\text{Frame Rate} = \frac{\frac{20\,\text{MHz}}{\text{PSELB}}}{\text{T1B} \times (\text{VBPDB} + \text{VFPDB} + \text{Vertical Scanning Lines})}$$</td></tr>
<tr><td>Restriction</td><td>T1B[9:0] ≥ 101h (257d)
VBPDB[7:0] ≥ 6, VFPDB[7:0] ≥ 6
VBPDB[7:0]+VFPDB[7:0]+Vertical Scan Lines = multiple of 4 if PRG=”0”</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>BE00h, BE01h (T1B)</th><th>BE02h (VBPDB)</th><th>BE03h (VFPDB)</th><th>BE04h (PSELB)</th></tr>
<tr><td>Power On Sequence</td><td>01h, 84h</td><td>1Ch</td><td>1Ch</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>01h, 84h</td><td>1Ch</td><td>1Ch</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>01h, 84h</td><td>1Ch</td><td>1Ch</td><td>00h</td></tr>
</table>
</td></tr>
</table>

DPFRCTR3: Display Timing Control in Partial / Idle Off Mode (Page 0, BF00h~BF04h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPFRCTR3	R/W	BFh	BF00h	00h	-	-	-	-	-	-	T1C9	T1C8
			BF01h	00h	T1C7	T1C6	T1C5	T1C4	T1C3	T1C2	T1C1	T1C0
			BF02h	00h	VBPDC 7	VBPDC 6	VBPDC 5	VBPDC 4	VBPDC 3	VBPDC 2	VBPDC 1	VBPDC 0
			BF03h	00h	VFPDC 7	VFPDC 6	VFPDC 5	VFPDC 4	VFPDC 3	VFPDC 2	VFPDC 1	VFPDC 0
			BF04h	00h	-	-	-	-	-	-	PSELC 1	PSELC 0

NOTE: "-" Don't care

Description

This command is used to set the display time of one scan line (Hsync), the vertical blanking porch line, and pixel clock frequency for display timing in partial / idle off.

T1C[9:0]: the display time of one scan line in partial / idle off mode.

T1C[9:0]	No. of Pixel Clock	Display Time for One Scan Line (Pixel Clock=20 MHz)
0d~256d	-	reserved
257d	258	12.90 µs
258d	259	12.95 µs
:	:	: (0.05 µs/Step)
388d	389	19.45 µs
:	:	: (0.05 µs/Step)
1022d	1023	51.15 µs
1023d	1024	51.20 µs

VBPDC[7:0]: the vertical back porch lines in partial / idle off mode.
VFPDC[7:0]: the vertical front porch lines in partial / idle off mode.

VBPDC[7:0]	No. of Vertical Porch Line	VFPDC[7:0]	No. of Vertical Porch Line
00h~01h	reserved	00h~01h	reserved
02h	2 lines	02h	2 lines
03h	3 lines	03h	3 lines
:	: (1 line/Step)	:	: (1 line/Step)
1Ch	28 lines	1Ch	28 lines
:	: (1 line/Step)	:	: (1 line/Step)
FEh	254 lines	FEh	254 lines
FFh	255 lines	FFh	255 lines

PSELC[1:0]: the pixel clock frequency selection in partial / idle off mode.

PSELC[1:0]	Divisor Condition
00h	1
01h	2
02h	4
03h	8

<table>
<tr><td>Description</td><td>The display frame frequency is decided by T1C[9:0] and this vertical porch lines as below.
$$\text{Frame Rate} = \frac{\frac{20\,\text{MHz}}{\text{PSELC}}}{\text{T1C} \times (\text{VBPDC} + \text{VFPDC} + \text{Vertical Scanning Lines})}$$</td></tr>
<tr><td>Restriction</td><td>T1C[9:0] ≥ 101h (257d)
VBPDC[7:0] ≥ 6, VFPDC[7:0] ≥ 6
VBPDC[7:0]+VFPDC[7:0]+Vertical Scan Lines = multiple of 4 if PRG=”0”</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>BF00h, BF01h (T1C)</th><th>BF02h (VBPDC)</th><th>BF03h (VFPDC)</th><th>BF04h (PSELC)</th></tr>
<tr><td>Power On Sequence</td><td>01h, 84h</td><td>1Ch</td><td>1Ch</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>01h, 84h</td><td>1Ch</td><td>1Ch</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>01h, 84h</td><td>1Ch</td><td>1Ch</td><td>00h</td></tr>
</table>
</td></tr>
</table>

DPTMCTR12: Display Timing Control 12 (Page 0, CC00h~CC02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPTMCTR12	R/W	CCh	CC00h	00h	-	-	-	LVGL_SEL_H	-	-	FHN	LR_H
			CC01h	00h	CLW_H7	CLW_H6	CLW_H5	CLW_H4	CLW_H3	CLW_H2	CLW_H1	CLW_H0
			CC02h	00h	FTI_H7	FTI_H6	FTI_H5	FTI_H4	FTI_H3	FTI_H2	FTI_H1	FTI_H0

NOTE: "-" Don't care

Description

This command is used to control display timing for VGSW[3:0]="1100".

LVGL_SEL: select LVGL voltage level.

LVGL_SEL	LVGL Voltage
0	VGLX
1	VGL_REG

FHN: select gate signal mode.

FHN	Gate Signal Mode
0	Non-overlape mode
1	Overlap mode

LR: output signal control for XXXX_R↔XXXX_L swap.

Pad Name	Output Signal	
	LR="0"	LR="1"
STP_O	STP_O	STP_E
CK_O	CK_O	CK_E
CKB_O	CKB_O	CKB_E
FW_L	FW_L	FW_R
BW_L	BW_L	BW_R
STP_E	STP_E	STP_O
CK_E	CK_E	CK_O
CKB_E	CKB_E	CKB_O
FW_R	FW_R	FW_L
BW_R	BW_R	BW_L

CLW_H[7:0]: delay time for CK_O/E and CKB_O/E signals

CLW_H[7:0]	No of Clock	Delay Time
00h	0	0.00μs
01h	1	0.05μs
02h	2	0.10μs
:	:	: (0.05μs/Step)
50h	80	4.00μs
:	:	: (0.05μs/Step)
FDh	253	12.65μs
FEh	254	12.70μs
FFh	255	12.75μs

Description

FTI_H[7:0]: delay time for STP_O/E signals

FTI_H[7:0]	No of Clock	Delay Time
00h	0	0.00µs
01h	1	0.05µs
02h	2	0.10µs
:	:	: (0.05µs/Step)
50h	80	4.00µs
:	:	: (0.05µs/Step)
FDh	253	12.65µs
FEh	254	12.70µs
FFh	255	12.75µs

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	CC00h	CC01h (CLW_H)	CC02h (FTI_H)
Power On Sequence	01h	50h	50h
S/W Reset	01h	50h	50h
H/W Reset	01h	50h	50h

LEDCTRDP: Control for LEDPWM/LEDON Pins (Page 0, D000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
LEDCTRDP	R/W	D0h	D000h	00h	-	-	LEDONR	LEDONPOL	LEDPWM_OEB	CLED_VOL	~~PWM_ENH_OE~~	LEDPWPOL

NOTE: "-" Don't care

Description

This command is used to control the voltage level, driving ability and active polarity of LEDON and LEDPWM pins.

LEDONR: the On/Off control for LEDON pin.

LEDONR	LEDONPOL	Status of LEDON Pin
0	0	Keep "Low"
0	1	Keep "High"
1	0	Keep "High"
1	1	Keep "Low"

LEDONPOL: the PWM active polarity for LEDON pin.

LEDONPOL	Polarity of LEDON Pin	
	Lit Period	Non-lit Period
0	High	Low
1	Low	High

LEDPWM_OEB: the enable control for LEDPWM pins.

C[1:0] (Command 5500h)	LEDPWM_OEB=0		LEDPWM_OEB=1
	LEDPWMPOL=0	LEDPWMPOL=1	
00, CABC off	High (100% duty)	Low (100% duty)	Hi-Z
01, UI mode	PWM waveform (active high)	PWM waveform (active low)	Hi-Z
10, Still mode			
11, Moving mode			

CLED_VOL: the voltage level for LEDON and LEDPWM pins.
This bit is valid when (1) DSTB_SEL=Low or (2) DSTB_SEL=High, VDDI=1.65~3.3V and VSEL=High . For other conditions, the output voltage level is DIOPWR depend on VDDI input voltage and VSEL (refer to the section Pin Description for VSEL pin).

CLED_VOL	Voltage Level of LEDON/LEDPWM Pins
0	VSSI to VDDI
1	VSSI to VDDA

LEDPWPOL: the PWM active polarity for LEDPWM pin.

LEDPWPOL	Polarity of LEDPWM Pin	
	Lit Period	Non-lit Period
0	High	Low
1	Low	High

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>D000h</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

DIMCTR: Dimming Control for LABC and CABC (Page 0, D200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTR	R/W	D2h	D200h	00h	-	-	-	-	SEL_IN	SEL_DE	-	-

NOTE: "-" Don't care

Description

This command is used to control the dimming method for LABC/CABC for display brightness.

SEL_IN: the rising dimming type for display brightness change by LABC function.

SEL_IN	Rising Dimming Type for LABC
0	"Fixed Time" type
1	"Fixed Slope" type

SEL_DE: the falling dimming type for display brightness change by LABC function.

SEL_DE	Falling Dimming Type for LABC
0	"Fixed Time" type
1	"Fixed Slope" type

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	D200h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

DIMCTRDP1: Display Brightness Dimming Control 1 for LABC and CABC (Page 0, D300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRDP1	R/W	D3h	D300h	00h	DM_IN3	DM_IN2	DM_IN1	DM_IN0	DM_DE3	DM_DE2	DM_DE1	DM_DE0

NOTE: "-" Don't care

Description

This command is used to control the time per dimming step for fixed-time / fixed-slope type dimming method which used for display brightness change by LABC and CABC.

DM_IN[3:0]: the time of each rising dimming step for Fixed-Time type and Fixed-Slope type.
DM_DE[3:0]: the time of each falling dimming step for Fixed-Time type and Fixed-Slope type.

DM_IN[3:0]	Time of Rising Dimming Step	DM_DE[3:0]	Time of Rising Dimming Step
0h	1 frame	0h	1 frame
1h	2 frames	1h	2 frames
2h	3 frames	2h	3 frames
:	:	:	:
Bh	12 frames	Bh	12 frames
Ch	13 frames	Ch	13 frames
Dh	14 frames	Dh	14 frames
Eh~Fh	reserved	Eh~Fh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	D300h (DM_IN, DM_DE)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

DIMCTRDP2: Display Brightness Dimming Control 2 for LABC and CABC (Page 0, D400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRDP2	R/W	D4h	D400h	00h	-	-	-	-	-	DMSTP_L2	DMSTP_L1	DMSTP_L0

NOTE: "-" Don't care

Description

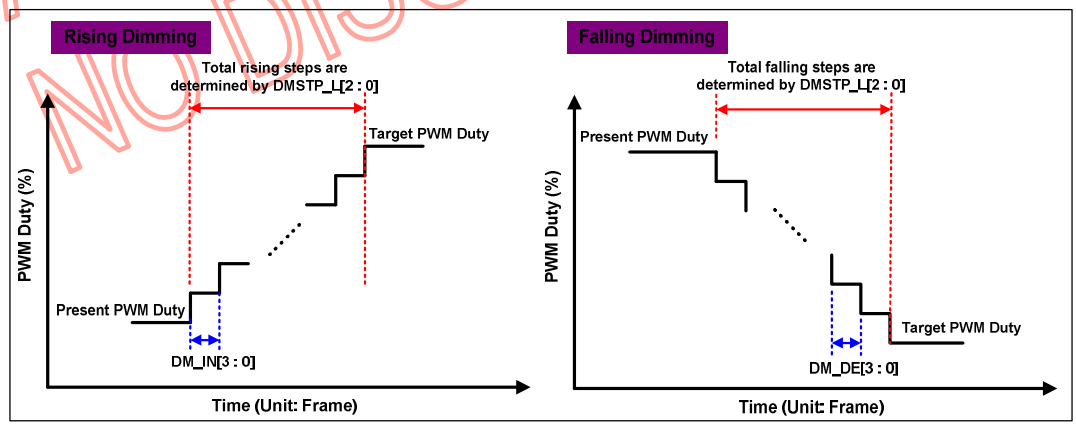
This command is used to control the total dimming steps for fixed-time type dimming method which used for display brightness change by LABC and CABC.

DMSTP_L[2:0]: the total rising/falling dimming steps for Fixed-Time type in Off-Mode and UI-Mode of CABC.

DMSTP_L[2:0]	Total Steps of Rising/Falling Dimming
0h	2 steps
1h	4 steps
2h	8 steps
3h	16 steps
4h	32 steps
5h	64 steps
6h	128 steps
7h	256 steps

Note: The setting of DMSTP_L[2:0] is available when dimming type is set to "Fixed-Time" type and CABC is set to "Off-Mode" and "UI-Mode".

Fixed-Time Type dimming in Off-Mode and UI-Mode



Example 1:
DM_IN[3:0] is set to 0x03 and DMSTP_L[2:0] is set to 0x06, this means that the time of each rising dimming step is 4 frames and 128 total dimming steps.
So the total dimming time length is 128x4=512 frames for LABC and CABC Off-Mode/UI-Mode.
Example 2:
DM_DE[3:0] is set to 0x04 and DMSTP_L[2:0] is set to 0x03, this means that the time of each falling dimming step is 5 frames and 16 total dimming steps.
So the total dimming time length is 16x5=80 frames for LABC and CABC Off-Mode/UI-Mode.

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>D400h (DMSTP_L)</th></tr>
<tr><td>Power On Sequence</td><td>04h</td></tr>
<tr><td>S/W Reset</td><td>04h</td></tr>
<tr><td>H/W Reset</td><td>04h</td></tr>
</table>
</td></tr>
</table>

DIMCTRDP3: Display Brightness Dimming Control 3 for LABC and CABC (Page 0, D500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRDP3	R/W	D5h	D500h	00h	STEP _IN3	STEP _IN2	STEP _IN1	STEP _IN0	STEP _DE3	STEP _DE2	STEP _DE1	STEP _DE0

NOTE: "-" Don't care

Description

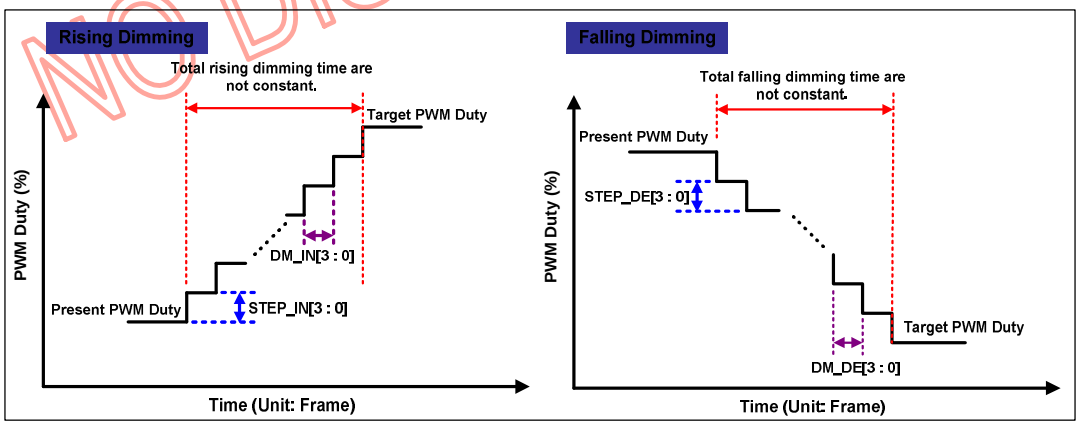
This command is used to control the brightness change per step for fixed-slope type dimming method which used for display brightness change by LABC and CABC.

STEP_IN[3:0]: the increment of PWM duty for rising dimming for Fixed-Slope type.
STEP_DE[3:0]: the decrement of PWM duty for falling dimming for Fixed-Slope type.

STEP_IN[3:0]	Increment of PWM Duty	STEP_DE[3:0]	Decrement of PWM Duty
0h	reserved	0h	reserved
1h	1	1h	1
2h	2	2h	2
3h	3	3h	3
:	:	:	:
Dh	13	Dh	13
Eh	14	Eh	14
Fh	15	Fh	15

Note: The setting of STEP_IN[3:0] and STEP_DE[3:0] are available when dimming type is set to "Fixed-Slope" type.

Fixed-Slope Type dimming



Example 1:
DM_IN[3:0] is set to 0x03 and STEP_IN[3:0] is set to 0x0E, this means that the PWM duty will increase 14 (around 14/256=5.47%) per 4 frames until the PWM duty reaches target PWM duty.
Example 2:
DM_DE[3:0] is set to 0x06 and STEP_DE[3:0] is set to 0x05, this means that the PWM duty will decrease 5 (around 5/256=1.95%) per 7 frames until the PWM duty reaches target PWM duty.

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>D500h (STEP_IN, STEP_DE)</th></tr>
<tr><td>Power On Sequence</td><td>11h</td></tr>
<tr><td>S/W Reset</td><td>11h</td></tr>
<tr><td>H/W Reset</td><td>11h</td></tr>
</table>
</td></tr>
</table>

DIMCTRCB2: Display Brightness Control 1 for LABC and CABC (Page 0, DD00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRCB2	R/W	DDh	DD00h	00h	-	DIM_ STEP_ MOV2	DIM_ STEP _MOV1	DIM_ STEP_ MOV0	-	DIM_ STEP_ STILL2	DIM_ STEP_ STILL1	DIM_ STEP_ STILL0

NOTE: "-" Don't care

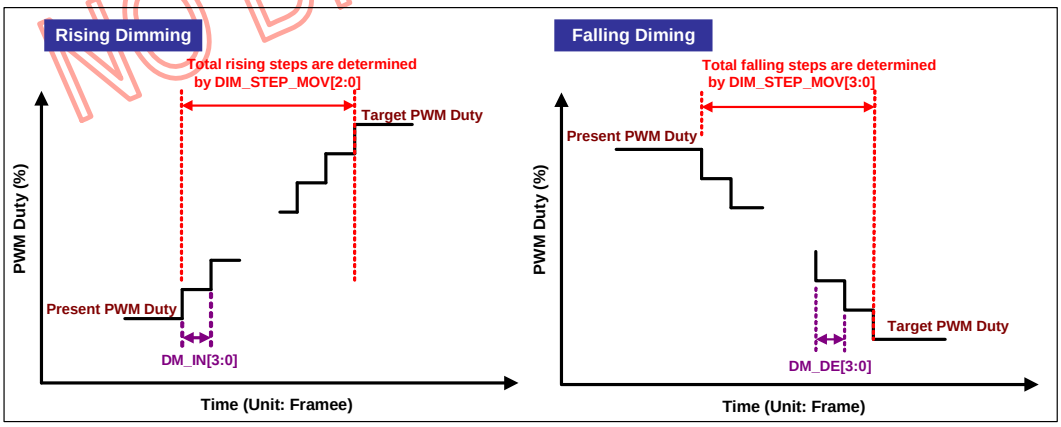
Description

This command is used to control the total dimming steps for fixed-time type dimming method which used for display brightness change by LABC and CABC (Moving-Mode and Still-Mode respectively).
DIMSTEP_MOV[2:0]: the total rising/falling dimming steps in Moving-Mode of CABC.
DIMSTEP_STILL[2:0]: the total rising/falling dimming steps in Still-Mode of CABC.

DIMSTEP_MOV[2:0]	Total Steps of Rising/Falling Dimming	DIMSTEP_STILL[2:0]	Total Steps of Rising/Falling Dimming
0h	2 steps	0h	2 steps
1h	4 steps	1h	4 steps
2h	8 steps	2h	8 steps
3h	16 steps	3h	16 steps
4h	32 steps	4h	32 steps
5h	64 steps	5h	64 steps
6h	128 steps	6h	128 steps
7h	256 steps	7h	256 steps

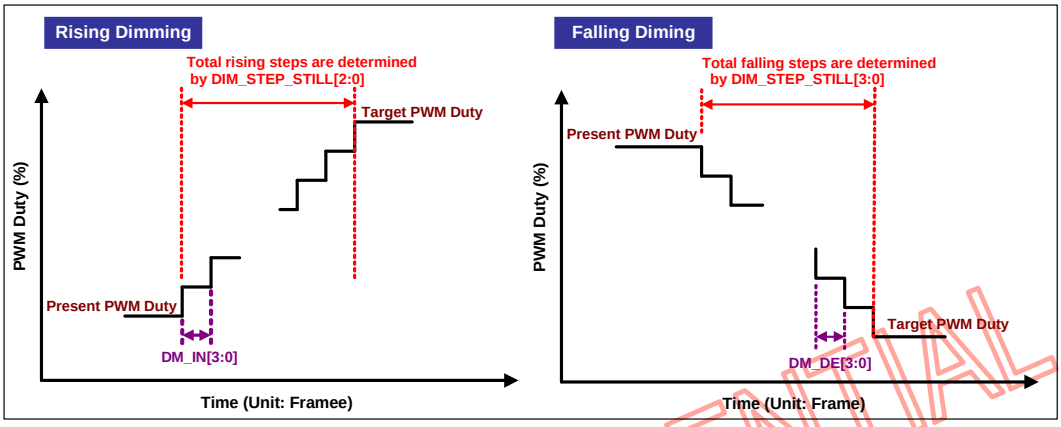
Note: The setting of DM_STEP_MOV[2:0] is available when dimming type is set to "Fixed-Time" type and CABC is set to "Moving-Mode". The setting of DM_STEP_STILL[2:0] is available when dimming type is set to "Fixed-Time" type and CABC is set to "Still-Mode".

Fixed-Time Type dimming in Moving-Mode



Description

Fixed-Time Type dimming in Still-Mode



Example 1:
DM_IN[3:0] and DM_DE[3:0] are set to 0x05 and DIM_STEP_MOV[2:0] is set to 0x01, this means that the time of each rising/falling dimming step is 6 frames and 4 total dimming steps.
So the total dimming time length is 4x6=24 frames for LABC and CABC Moving-Mode.
Example 2:
DM_IN[3:0] and DM_DE[3:0] are set to 0x01 and DIM_STEP_STILL[2:0] is set to 0x06, this means that the time of each rising/falling dimming step is 2 frames and 128 total dimming steps.
So the total dimming time length is 128x2=256 frames for LABC and CABC Still-Mode.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DD00h (DIM_STEP_MOV, DIM_STEP_STILL)
Power On Sequence	44h
S/W Reset	44h
H/W Reset	44h

PWMOFFDP: Offset Compensation for LEDPWM Pin (Page 0, DE00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PWMOFFDP	R/W	DEh	DE00h	00h	-	-	-	PWM_DUTY_OFFSET4	PWM_DUTY_OFFSET3	PWM_DUTY_OFFSET2	PWM_DUTY_OFFSET1	PWM_DUTY_OFFSET0

NOTE: "-" Don't care

Description

This command is used to compensate the effective PWM duty for LEDPWM pin.

PWM_DUTY_OFFSET[4:0]: compensate the effective PWM duty for LEDPWM pin.

PWM_DUTY_OFFSET[4:0]	PWM Duty Offset
0h	+0
1h	+1
:	:
3h	+30
4h	+31

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DE00h (PWM_DUTY_OFFSET)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

PWMFRCTR: PWM Frequency Control for LEDPWM Pin (Page 0, E000h~E002h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PWMFRCTR	R/W	E0h	E000h	00h	-	-	-	-	-	-	-	PWMF
			E001h	00h	PWM DIV7	PWM DIV6	PWM DIV5	PWM DIV4	PWM DIV3	PWM DIV2	PWM DIV1	PWM DIV0

NOTE: "-" Don't care

Description

This command is used to control the PWM clock frequency for LEDPWM pin.

PWMF: select the internal frequency source Fosc for generating the PWM signals.

PWMF	Fosc
0	5 MHz
1	10 MHz

PWMDIV[7:0]: the PWM frequency for LEDPWM pin.

$$\text{PWM Frequency} = \frac{\text{Fosc}}{256 \times \text{PWMDIV}[7:0]}$$

PWMF = "0"		PWMF = "1"	
PWMDIV[7:0]	PWM Frequency	PWMDIV[7:0]	PWM Frequency
00h	Setting Disabled	00h	Setting Disabled
01h	19.53 KHz	01h	39.06 KHz
02h	9.77 KHz	02h	19.53 KHz
03h	6.51 KHz	03h	13.02 KHz
:	:	:	:
FCh	77.50 Hz	FCh	155.01 Hz
FDh	77.20 Hz	FDh	154.40 Hz
FEh	76.89 Hz	FEh	153.79 Hz
FFh	76.59 Hz	FFh	153.19 Hz

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	E000h (PWMF)	E001h (PWMDIV)
Power On Sequence	00h	01h
S/W Reset	00h	01h
H/W Reset	00h	01h

FCBRTCB: Force Display Brightness for CABC (Page 0, E100h~E101h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
FCBRTCB	R/W	E1h	E100h	00h	-	-	-	-	-	-	-	FORCE_CABC_PWM
			E101h	00h	FORCE_CABC_DUTY7	FORCE_CABC_DUTY6	FORCE_CABC_DUTY5	FORCE_CABC_DUTY4	FORCE_CABC_DUTY3	FORCE_CABC_DUTY2	FORCE_CABC_DUTY1	FORCE_CABC_DUTY0

NOTE: "-" Don't care

Description

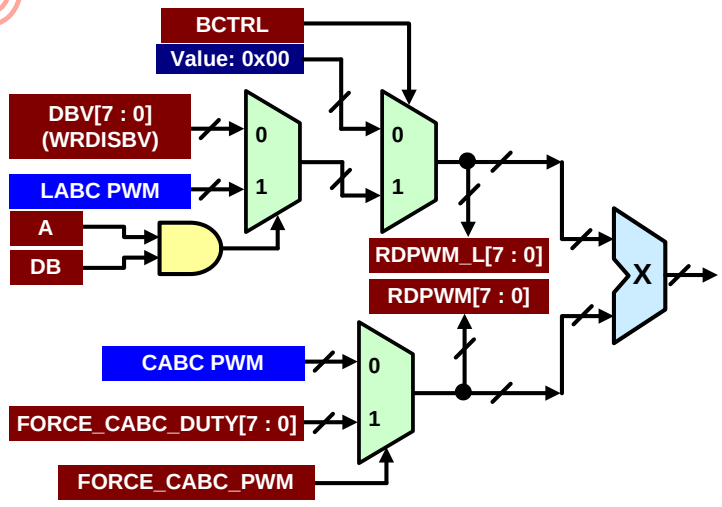
This command is used to force the CABC display brightness regardless the display content.

FORCE_CABC_PWM: force the CABC display brightness as the setting of FORCE_CABC_DUTY[7:0].

Bit	Description	Value
FORCE_CABC_PWM	Force CABC PWM duty enable/disable	"0": Force CABC PWM duty disable. CABC PWM duty is decided by CABC algorithm.
		"1": Force CABC PWM duty enable. CABC PWM duty is set by FORCE_CABC_DUTY[7:0].

FORCE_CABC_DUTY[7:0]: the setting display brightness of CABC when FORCE_CABC_PWM="1".

FORCE_CABC_DUTY[7:0]	Display Brightness of CABC
0h	Off
1h	2/256
2h	3/256
:	:
FDh	254/256
FEh	255/256
FFh	1



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<tr><th>E100h (FORCE_CABC_PWM)</th><th>E101h (FORCE_CABC_DUTY)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>FFh</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>FFh</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>FFh</td></tr>
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</table>

BRTCBUI: Display Brightness Control for CABC UI-Mode (Page 0, E200h~E203h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BRTCBUI	R/W	E2h	E200h	00h	CABC_UI_PWM07	CABC_UI_PWM06	CABC_UI_PWM05	CABC_UI_PWM04	CABC_UI_PWM03	CABC_UI_PWM02	CABC_UI_PWM01	CABC_UI_PWM00
			E201h	00h	CABC_UI_PWM17	CABC_UI_PWM16	CABC_UI_PWM15	CABC_UI_PWM14	CABC_UI_PWM13	CABC_UI_PWM12	CABC_UI_PWM11	CABC_UI_PWM10
			E202h	00h	CABC_UI_PWM27	CABC_UI_PWM26	CABC_UI_PWM25	CABC_UI_PWM24	CABC_UI_PWM23	CABC_UI_PWM22	CABC_UI_PWM21	CABC_UI_PWM20
			E203h	00h	CABC_UI_PWM37	CABC_UI_PWM36	CABC_UI_PWM35	CABC_UI_PWM34	CABC_UI_PWM33	CABC_UI_PWM32	CABC_UI_PWM31	CABC_UI_PWM30

NOTE: "-" Don't care

Description

This command is used to control the display brightness corresponding to different gamma algorithm in CABC UI-Mode.

The CABC UI-Mode is used to keep the good display quality and brightness, so the variance s of display brightness and estimated gamma curve are small. In other words, base on different image content, the CABC function will determine a better display brightness and estimated gamma curve in order to keep the approximated display brightness and quality.

The display brightness can be calculated by below.

$$\text{Display Brightness} = \frac{\text{CABC\_UI\_PWMn}[7:0] + 1}{256}$$

For example:

If CABC_UI_PWM0[7:0] is set to 0xF3, the display brightness for this setting will be

$$\text{Display Brightness} = \frac{243 + 1}{256} \approx 95.3\%$$

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	E200h	E201h	E202h	E203h
Power On Sequence	F3h	ECh	E7h	DFh
S/W Reset	F3h	ECh	E7h	DFh
H/W Reset	F3h	ECh	E7h	DFh

BRTCBSTL: Display Brightness Control for CABC Still-Mode (Page 0, E300h~E309h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BRTCBSTL	R/W	E3h	E300h	00h	CABC_ PWM07	CABC_ PWM06	CABC_ PWM05	CABC_ PWM04	CABC_ PWM03	CABC_ PWM02	CABC_ PWM01	CABC_ PWM00
			E301h	00h	CABC_ PWM17	CABC_ PWM16	CABC_ PWM15	CABC_ PWM14	CABC_ PWM13	CABC_ PWM12	CABC_ PWM11	CABC_ PWM10
			E302h	00h	CABC_ PWM27	CABC_ PWM26	CABC_ PWM25	CABC_ PWM24	CABC_ PWM23	CABC_ PWM22	CABC_ PWM21	CABC_ PWM20
			E303h	00h	CABC_ PWM37	CABC_ PWM36	CABC_ PWM35	CABC_ PWM34	CABC_ PWM33	CABC_ PWM32	CABC_ PWM31	CABC_ PWM30
			E304h	00h	CABC_ PWM47	CABC_ PWM46	CABC_ PWM45	CABC_ PWM44	CABC_ PWM43	CABC_ PWM42	CABC_ PWM41	CABC_ PWM40
			E305h	00h	CABC_ PWM57	CABC_ PWM56	CABC_ PWM55	CABC_ PWM54	CABC_ PWM53	CABC_ PWM52	CABC_ PWM51	CABC_ PWM50
			E306h	00h	CABC_ PWM67	CABC_ PWM66	CABC_ PWM65	CABC_ PWM64	CABC_ PWM63	CABC_ PWM62	CABC_ PWM61	CABC_ PWM60
			E307h	00h	CABC_ PWM77	CABC_ PWM76	CABC_ PWM75	CABC_ PWM74	CABC_ PWM73	CABC_ PWM72	CABC_ PWM71	CABC_ PWM70
			E308h	00h	CABC_ PWM87	CABC_ PWM86	CABC_ PWM85	CABC_ PWM84	CABC_ PWM83	CABC_ PWM82	CABC_ PWM81	CABC_ PWM80
			E309h	00h	CABC_ PWM97	CABC_ PWM96	CABC_ PWM95	CABC_ PWM94	CABC_ PWM93	CABC_ PWM92	CABC_ PWM91	CABC_ PWM90

NOTE: "-" Don't care

Description	This command is used to set the display brightness corresponding to different gamma algorithm in CABC Still-Mode. Base on different image content, the CABC function will determine a better display brightness and estimated gamma curve in order to keep the approximated display brightness and quality. The display brightness can be calculated by below. $\text{Display Brightness} = \frac{\text{CABC\_PWMn}[7:0]+1}{256}$ For example: If CABC_UI_PWM0[7:0] is set to 0x99, the display brightness for this setting will be $\text{Display Brightness} = \frac{153+1}{256} \approx 60.2\%$

<table>
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<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
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<tr><td>Power On Sequence</td><td>F3h</td><td>D9h</td><td>CCh</td><td>C0h</td><td>B3h</td><td>A6h</td><td>99h</td><td>99h</td><td>99h</td><td>95h</td></tr>
<tr><td>S/W Reset</td><td>F3h</td><td>D9h</td><td>CCh</td><td>C0h</td><td>B3h</td><td>A6h</td><td>99h</td><td>99h</td><td>99h</td><td>95h</td></tr>
<tr><td>H/W Reset</td><td>F3h</td><td>D9h</td><td>CCh</td><td>C0h</td><td>B3h</td><td>A6h</td><td>99h</td><td>99h</td><td>99h</td><td>95h</td></tr>
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</td></tr>
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BRTCBMOV: Display Brightness Control for CABC Moving-Mode (Page 0, E400h~E409h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BRTCBMOV	R/W	E4h	E400h	00h	CABC_MOV_PWM07	CABC_MOV_PWM06	CABC_MOV_PWM05	CABC_MOV_PWM04	CABC_MOV_PWM03	CABC_MOV_PWM02	CABC_MOV_PWM01	CABC_MOV_PWM00
			E401h	00h	CABC_MOV_PWM17	CABC_MOV_PWM16	CABC_MOV_PWM15	CABC_MOV_PWM14	CABC_MOV_PWM13	CABC_MOV_PWM12	CABC_MOV_PWM11	CABC_MOV_PWM10
			E402h	00h	CABC_MOV_PWM27	CABC_MOV_PWM26	CABC_MOV_PWM25	CABC_MOV_PWM24	CABC_MOV_PWM23	CABC_MOV_PWM22	CABC_MOV_PWM21	CABC_MOV_PWM20
			E403h	00h	CABC_MOV_PWM37	CABC_MOV_PWM36	CABC_MOV_PWM35	CABC_MOV_PWM34	CABC_MOV_PWM33	CABC_MOV_PWM32	CABC_MOV_PWM31	CABC_MOV_PWM30
			E404h	00h	CABC_MOV_PWM47	CABC_MOV_PWM46	CABC_MOV_PWM45	CABC_MOV_PWM44	CABC_MOV_PWM43	CABC_MOV_PWM42	CABC_MOV_PWM41	CABC_MOV_PWM40
			E405h	00h	CABC_MOV_PWM57	CABC_MOV_PWM56	CABC_MOV_PWM55	CABC_MOV_PWM54	CABC_MOV_PWM53	CABC_MOV_PWM52	CABC_MOV_PWM51	CABC_MOV_PWM50
			E406h	00h	CABC_MOV_PWM67	CABC_MOV_PWM66	CABC_MOV_PWM65	CABC_MOV_PWM64	CABC_MOV_PWM63	CABC_MOV_PWM62	CABC_MOV_PWM61	CABC_MOV_PWM60
			E407h	00h	CABC_MOV_PWM77	CABC_MOV_PWM76	CABC_MOV_PWM75	CABC_MOV_PWM74	CABC_MOV_PWM73	CABC_MOV_PWM72	CABC_MOV_PWM71	CABC_MOV_PWM70
			E408h	00h	CABC_MOV_PWM87	CABC_MOV_PWM86	CABC_MOV_PWM85	CABC_MOV_PWM84	CABC_MOV_PWM83	CABC_MOV_PWM82	CABC_MOV_PWM81	CABC_MOV_PWM80
			E409h	00h	CABC_MOV_PWM97	CABC_MOV_PWM96	CABC_MOV_PWM95	CABC_MOV_PWM94	CABC_MOV_PWM93	CABC_MOV_PWM92	CABC_MOV_PWM91	CABC_MOV_PWM90

NOTE: "-" Don't care

Description	This command is used to set the display brightness corresponding to different gamma algorithm in CABC Moving-Mode. Base on different image content, the CABC function will determine a better display brightness and estimated gamma curve in order to keep the approximated display brightness and quality. The display brightness can be calculated by below. $\text{Display Brightness} = \frac{\text{CABC\_MOV\_PWMn[7:0]} + 1}{256}$ For example: If CABC_UI_PWM0[7:0] is set to 0xB3, the display brightness for this setting will be $\text{Display Brightness} = \frac{179 + 1}{256} \approx 70.3\%$

<table>
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<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
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<tr><td>S/W Reset</td><td>F3h</td><td>D9h</td><td>CCh</td><td>C0h</td><td>B3h</td><td>A6h</td><td>99h</td><td>99h</td><td>99h</td><td>95h</td></tr>
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AMOVCTR: Automatic Moving-Mode Detection Control (Page 0, E500h~E501h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
AMOVCTR	R/W	E5h	E500h	00h	-	MOV DET6	MOV DET5	MOV DET4	MOV DET3	MOV DET2	MOV DET1	MOV DET0
			E501h	00h	-	-	-	MOV SC4	MOV SC3	MOV SC2	MOV SC1	MOV SC0

NOTE: "-" Don't care

Description

This command is used to set the condition for automatic Moving-Mode selection for CABC.
The Moving-Mode means that the frame memory is continuously updated for displaying. The CABC function provides three CABC modes – UI-Mode, Still-Mode and Moving-Mode. This function is only available in Normal Display Mode (command NORON) with CABC mode is set to Still-Mode (C[1:0] of command 5500h is "10"). In other words, the "Moving-Mode Detection" function does not work when CABC has been set in UI-Mode (C[1:0] of command 5500h is "01") or Moving-Mode (C[1:0] of command 5500h is "11").

MOVDET[6:0]: the frame memory updated rate for Moving-Mode detection.
This setting is applied to set a period which the driver IC will monitor frame memory updating rate each specified period. This function is turned off when MOVDET[6:0] is set to "00h".

MOVDET[6:0]	Detection Condition
0h	Moving-Mode detection disable
1h	2 frames
2h	3 frames
3h	4 frames
:	:
7Dh	126 frames
7Eh	127 frames
7Fh	128 frames

For example:
If MOVDET[6:0] is set to 0x0A, this means the driver IC will check frame memory updated rate each 10-frame time period..

<table>
<tr><td>Description</td><td>
MOVSC[4:0]: set the de-bounce times of frame memory updated each specified time.
There is an internal counter to calculate how many time does frame memory has been updated each specified time period. If the frame memory has been updated (even only been updated one time) each specified time length, the internal counter will increase 1. Otherwise, if the frame memory has not been updated any time each specified time length, the internal counter will decrease 1.
Finally, if the value of internal counter larger than the value of MOVSC[4:0], the CABC mode will be changed from “Still-Mode” to “Moving-Mode” automatically. If the value of internal counter equals to 0, the CABC mode will be changed from “Moving-Mode” to “Still-Mode”.
<table>
<tr><th>MOVSC[4:0]</th><th>De-bounce Times</th></tr>
<tr><td>00h</td><td>1 time</td></tr>
<tr><td>01h</td><td>2 times</td></tr>
<tr><td>02h</td><td>3 times</td></tr>
<tr><td>03h</td><td>4 times</td></tr>
<tr><td>04h</td><td>5 times</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>1Dh</td><td>30 times</td></tr>
<tr><td>1Eh</td><td>31 times</td></tr>
<tr><td>1Fh</td><td>32 times</td></tr>
</table>
For example:
If host ‘s frame memory updated rate is once per 10 frames, then set MOVDET[7:0] to 0x0A. And set MOVSC[4:0] as 0x06 for de-bounce 6 times to avoid the non-moving frame memory writing be detected. Whenever frame memory updated within each 10 frames, the internal counter will increase 1. Until the value of internal counter equal to 6 (MOVSC[4:0]), the CABC mode will be changed from “Still-Mode” to “Moving-Mode” automatically.
However, if the frame memory updated rate is 1 stopped per 12 frames, this means the frame memory will be updated 0.83 time during 10 frames period (MOVDET[6:0]), the internal counter will decrease 1 every 20 frames. Until the value of internal counter equals to 0, the CABC mode will be changed from “Moving-Mode” to “Still-Mode”.
</td></tr>
<tr><td>Restriction</td><td>Only available in Normal Display Mode with CABC mode is set in “Still-Mode”.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>E500h (MOVDET)</th><th>E501h (MOVSC)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>04h</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>04h</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>04h</td></tr>
</table>
</td></tr>
</table>

FHYSTCTR: Final Hsyteresis Result Control (Page 0, E600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
FHYSTCTR	R/W	E6h	E600h	00h	SET_ HYST	-	-	-	HYST_ OUT_ VAL3	HYST_ OUT_ VAL2	HYST_ OUT_ VAL1	HYST_ OUT_ VAL0

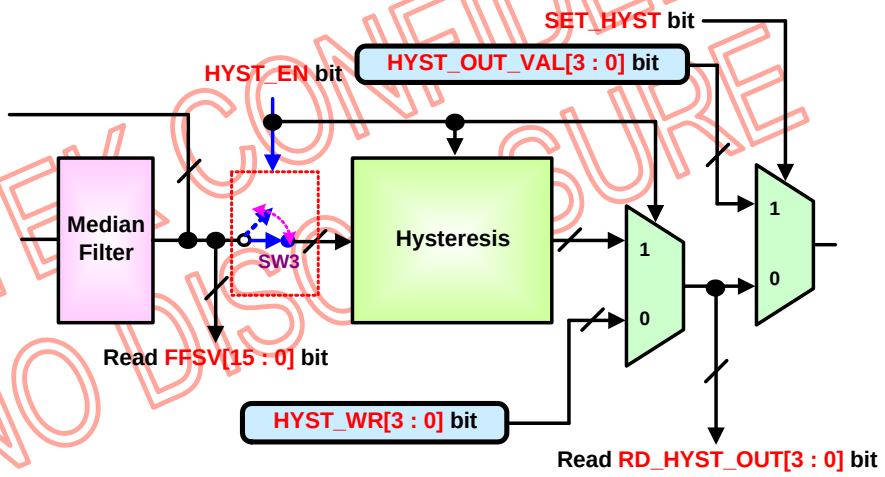
NOTE: "-" Don't care

Description

This command is used to control the final hysteresis result for LABC.

SET_HYST: select the final hysteresis result regardless the internal hysteresis function is enable or not.
HYST_OUT_VAL[3:0]: set the final hysteresis result when SET_HYST="1"

SET_HYST	HYST_EN	Final Hysteresis Result
0	0	HYST_WR[3:0]
	1	Internal hysteresis result
1	X	HYST_OUT_VAL[3:0]



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	E600h (SET_HYST, HYST_OUT_VAL)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

HYSTCTR: Internal Hsyteresis Function Control (Page 0, E700h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
HYSTCTR	R/W	E7h	E700h	00h	HYST_EN	-	-	-	HYST_WR3	HYST_WR2	HYST_WR1	HYST_WR0

NOTE: "-" Don't care

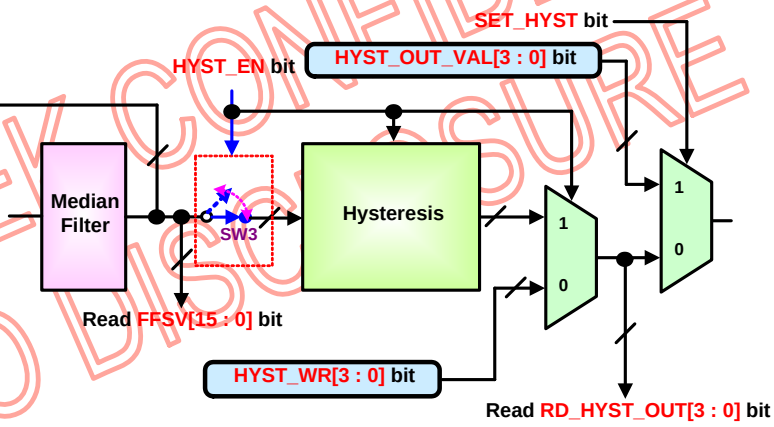
Description

This command is used to control the internal hysteresis function for LABC.

HYST_EN: enable/disable the internal hsyteresis function.
HYST_WR[3:0]: set the specified hysteresis result when HYST_EN="0".

HYST_EN	Internal Hysteresis Function
0	Disable
1	Enable

The external host can set HYST_EN="0" to disable internal hysteresis function and do hysteresis by external host itself. Based on the read value of register FFSV[15:0], the external host can write its hysteresis result into HYST_WR[3:0] to specified the hysteresis result.



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	E700h (HYST_EN, HYST_WR)
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

FLTCTR: Median Filter and Flicker Filter Control (Page 0, E800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
FLTCTR	R/W	E8h	E800h	00h	MRF_ BYS	-	-	-	FKP3	FKP2	FKP1	FKP0

NOTE: "-" Don't care

Description

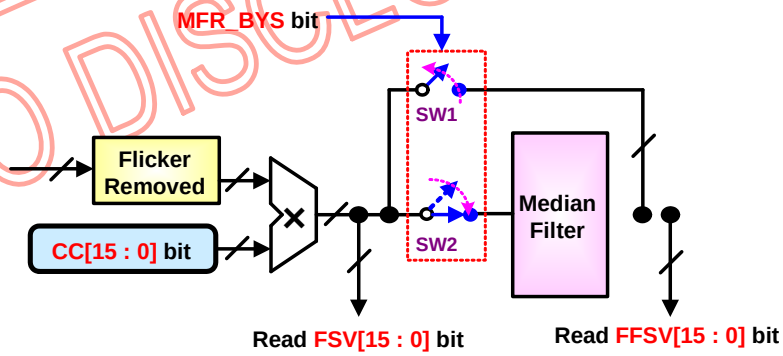
This command is used to control the internal Median Filter and internal Flicker Filter for LABC.

MRF_BYS: decide the value of register FSV[15:0] to pass or bypass the internal Median Filter.

MRF_BYS	Value of FSSV[15:0]
0	FSV[15:0] proceeded by Median Filter
1	Equal to FSV[15:0]

FKP[3:0]: the averaging time period for Flicker Filter.

FKP[3:0]	Averaging Time Period for Flicker Filter
0h	0.2 sec
1h	0.4 sec
2h	0.6 sec
:	: (0.2 sec/Step)
Dh	2.8 sec
Eh	3.0 sec
Fh	Reserved



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<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>E800h (MRF_BYS, FKP)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

WRALSV: Write Ambient Light Information (Page 0, E900h~E902h)

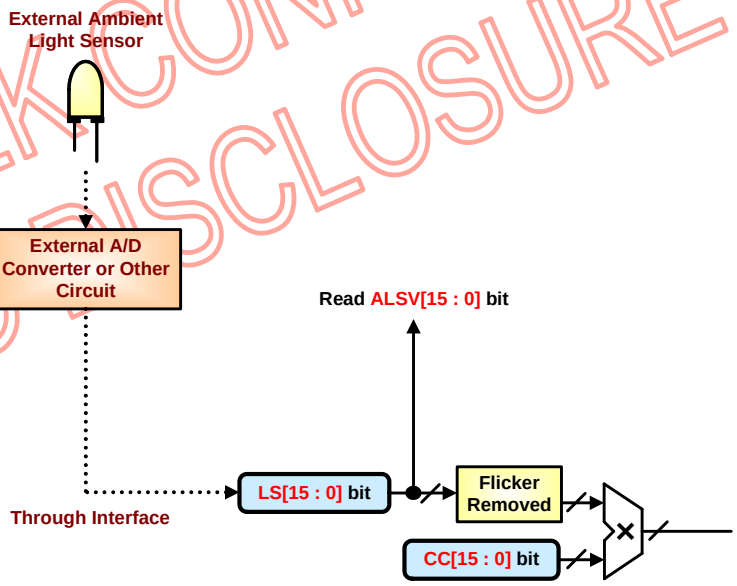
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRALSV	R/W	E9h	E900h	00h	LS7	LS6	LS5	LS4	LS3	LS2	LS1	LS0
			E901h	00h	LS15	LS14	LS13	LS12	LS11	LS10	LS9	LS8
			E902h	00h	-	-	-	-	-	-	-	ALS_W

NOTE: "-" Don't care

Description

This command is used to write the given ambient light information into LABC circuit.

LS[7:0]: the LSBs of ambient light information.
LS[15:0]: the MSBs of ambient light information.
ALS_W: send the ambient light information LS[15:0] into the internal circuit.
The step to write ambient light information LS[15:0]
Step 1: First, write the value into register LS[7:0] for updating the LSBs of LS[15:0].
Step 2: Second, write the value into register LS[15:8] for updating the MSBs of LS[15:0].
Step3: Finally, set the register bit ALS_W="1", then the value of LS[15:0] will be completely send into the internal circuit. The bit ALS_W becomes "0" after LS[15:0] is written completely.



<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>E900h, E901h (LS)</th><th>E902h (ALS_W)</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>00h</td></tr>
</table>
</td></tr>
</table>

RDBRTDPL: Read Display Brightness from LABC (Page 0, EA00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBRTDPL	R	EAh	EA00h	00h	RDPWM_L7	RDPWM_L6	RDPWM_L5	RDPWM_L4	RDPWM_L3	RDPWM_L2	RDPWM_L1	RDPWM_L0

NOTE: "-" Don't care

Description

This command is used to read the display brightness value which proceeded by LABC blocks.

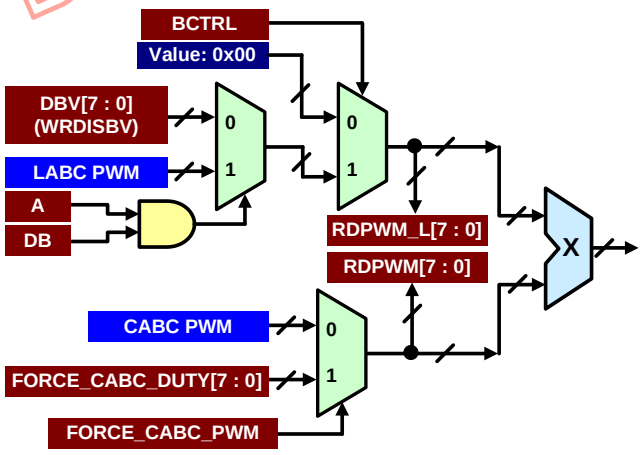
RDPWM_L[7:0]: the display brightness value from LABC block.

RDPWM_L[7:0]	PWM Duty for Display from LABC
00h	Off
01h	2/256
02h	3/256
:	:
FDh	254/256
FEh	255/256
FFh	1

The below table lists the relation between LABC output and DBV[7:0] (here means from WRDISBV command).

Register bit "A"	Register bit "DB"	RDPWM_L[7:0]
0	0	DBV[7:0] (here means from WRDISBV command)
0	1	DBV[7:0] (here means from WRDISBV command)
1	0	DBV[7:0] (here means from WRDISBV command)
1	1	Display Brightness Value by LABC Modified

Display brightness control block combined with LABC and CABC



<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>EA00h (RDPWM_L)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

RDBRTDPC: Read Display Brightness from CABC (Page 0, EB00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBRTDPL	R	EBh	EB00h	00h	RDPWM 7	RDPWM 6	RDPWM 5	RDPWM 4	RDPWM 3	RDPWM 2	RDPWM 1	RDPWM 0

NOTE: "-" Don't care

Description

This command is used to read the display brightness value which proceeded by CABC blocks.

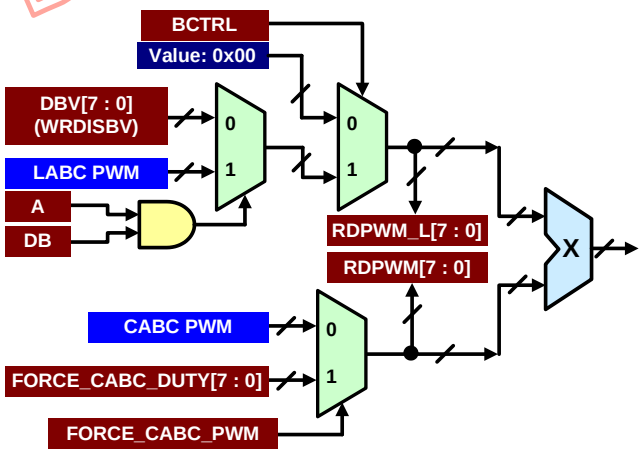
RDPWM[7:0]: the display brightness value from CABC block.

RDPWM[7:0]	PWM Duty for Display from CABC
00h	Off
01h	2/256
02h	3/256
:	:
FDh	254/256
FEh	255/256
FFh	1

The below table lists the relation between CABC output and RDPWM[7:0].

FORCE_CABC_PWM="0"		FORCE_CABC_PWM="1"	
CABC Mode	RDPWM[7:0]	CABC Mode	RDPWM[7:0]
Off-Mode	FFh	Off-Mode	FORCE_CABC_DUTY[7:0]
UI-Mode	Value by CABC Modified	UI-Mode	FORCE_CABC_DUTY[7:0]
Still-Mode	Value by CABC Modified	Still-Mode	FORCE_CABC_DUTY[7:0]
Moving-Mode	Value by CABC Modified	Moving-Mode	FORCE_CABC_DUTY[7:0]

Display brightness control block combined with LABC and CABC



<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td rowspan="2">Status</td><td>Default Value</td></tr>
<tr><td>EB00h (RDPWM)</td></tr>
<tr><td>Power On Sequence</td><td>FFh</td></tr>
<tr><td>S/W Reset</td><td>FFh</td></tr>
<tr><td>H/W Reset</td><td>FFh</td></tr>
</table>
</td></tr>
</table>

RDHYST: Read Hysteresis Result (Page 0, ED00h)

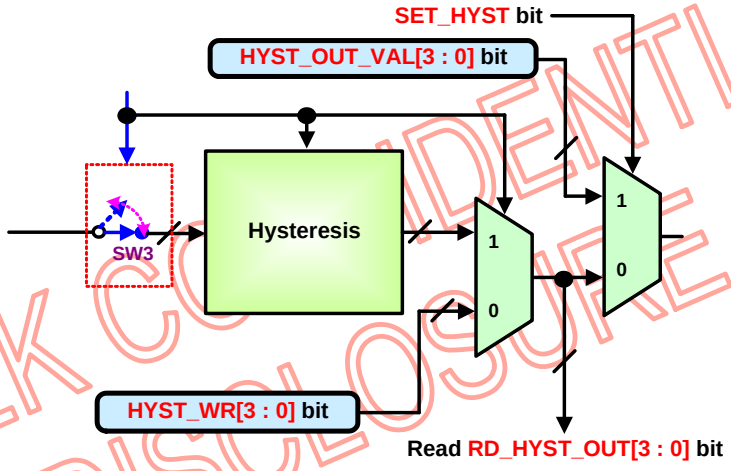
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDHYST	R	EDh	ED00h	00h	-	-	-	-	RD_HYST_OUT3	RD_HYST_OUT2	RD_HYST_OUT1	RD_HYST_OUT0

NOTE: "-" Don't care

Description

This command is used to read the hysteresis result from the output of internal hysteresis function block of LABC.

RD_HYST_OUT[3:0]: the hysteresis result from the output of hysteresis function block.



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	ED00h (RD_HYST_OUT)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

RDGMA: Read Gamma Curve (Page 0, EE00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGMA	R	EEh	EE00h	00h	RD_GMA_SET7	RD_GMA_SET6	RD_GMA_SET5	RD_GMA_SET4	RD_GMA_SET3	RD_GMA_SET2	RD_GMA_SET1	RD_GMA_SET0

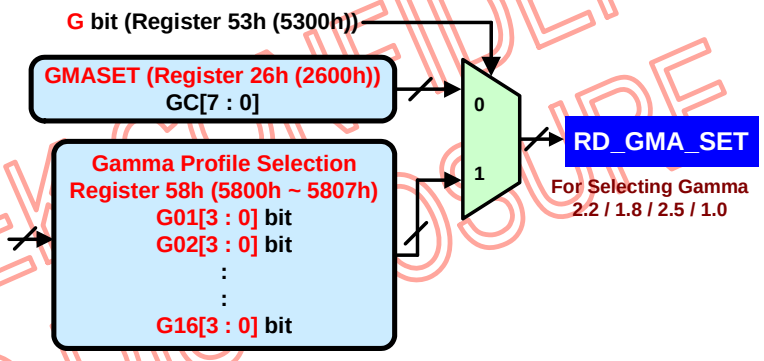
NOTE: "-" Don't care

Description

This command is used to read the gamma curve for the current display which proceeded by LABC.

RD_GMA_SET[7:0]: the gamma curve for the current display.

RD_GMA_SET[7:0]	Gamma Curve for Current Display
01h	Gamma Curve 1 (G=2.2)
02h	Gamma Curve 2 (G=1.8)
04h	Gamma Curve 3 (G=2.5)
08h	Gamma Curve 4 (G=1.0)



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	EE01h (RD_GMA_SET)
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

RDALSV: Read Ambient Light Information (Page 0, EF00h~EF01h)

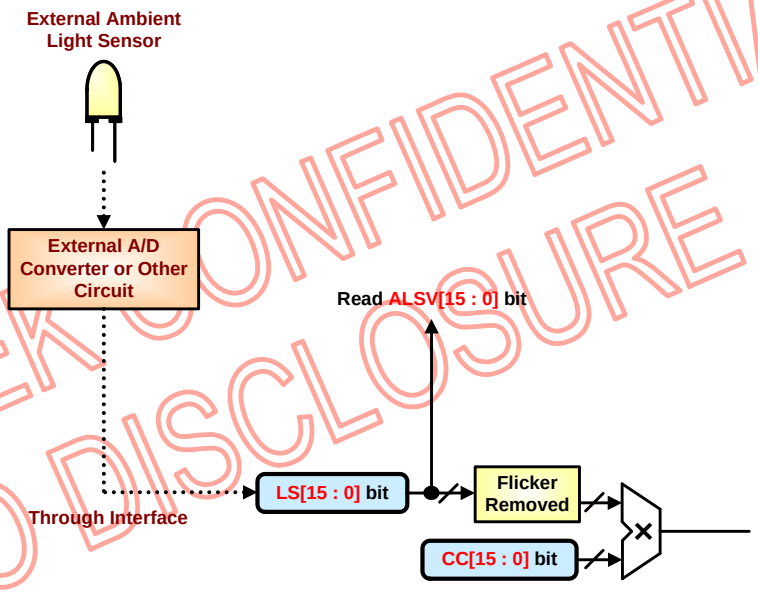
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDALSV	R	EFh	EF00h	00h	ALSV7	ALSV6	ALSV5	ALSV4	ALSV3	ALSV2	ALSV1	ALSV0
			EF01h	00h	ALSV15	ALSV14	ALSV13	ALSV12	ALSV11	ALSV10	ALSV9	ALSV8

NOTE: "-" Don't care

Description

This command is used to read the ambient light information which sent into LABC.

ALSV[7:0]: the LSBs of ambient light information.
ALSV[15:0]: the MSBs of ambient light information.



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	EF00h, EF01 (ALSV)
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

1.3 Manufacture Command Set for Page 1

Table 1.3.1 Manufacture Command Set – Page 1

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
SETAVDD	Dir	R/W	B0h	B000h	00h	-	-	-	VBPA[4:0]					Set AVDD voltage
				B001h	00h				VBPB[4:0]					
				B002h	00h				VBPC[4:0]					
SETAVEE	Dir	R/W	B1h	B100h	00h	-	-	-	VBNA[4:0]					Set AVEE voltage
				B101h	00h	-	-	-	VBNB[4:0]					
				B102h	00h	-	-	-	VBNC[4:0]					
SETVCL	Dir	R/W	B2h	B200h	00h	-	-	-	-	-	-	VBCLA[1:0]		Set VCL voltage
				B201h	00h	-	-	-	-	-	-	VBCLB[1:0]		
				B202h	00h	-	-	-	-	-	-	VBCLC[1:0]		
SETVGH	Dir	R/W	B3h	B300h	00h	-	-	-	-	VBHA[3:0]				Set VGH voltage
				B301h	00h	-	-	-		VBHB[3:0]				
				B302h	00h	-	-	-	-	VBHC[3:0]				
SETVRGH	Dir	R/W	B4h	B400h	00h	-	-	VRGHA[5:0]						Set VRGH voltage
				B401h	00h	-	-	VRGHB[5:0]						
				B402h	00h	-	-	VRGHC[5:0]						
SETVGL_REG	Dir	R/W	B5h	B500h	00h	-	-	-	-	VBLA[3:0]				Set VGL_REG voltage
				B501h	00h	-	-			VBLB[3:0]				
				B502h	00h	-	-	-	-	VBLC[3:0]				
BT1CTR	Dir	R/W	B6h	B600h	00h	-	BTPA[2:0]			-	PCKA[2:0]			Set AVDD boosting times/frequency
				B601h	00h	-	BTPB[2:0]			-	PCKB[2:0]			
				B602h	00h	-	BTPC[2:0]			-	PCKC[2:0]			
BT2CTR	Dir	R/W	B7h	B700h	00h	-	BTNA[2:0]			-	NCKA[2:0]			Set AVEE boosting times/frequency
				B701h	00h	-	BTNB[2:0]			-	NCKB[2:0]			
				B702h	00h	-	BTNC[2:0]			-	NCKC[2:0]			
BT3CTR	Dir	R/W	B8h	B800h	00h	-	BTCLA [1:0]			-	CLCKA[2:0]			Set VCL boosting times/frequency
				B801h	00h	-	BTCLB [1:0]			-	CLCKB[2:0]			
				B802h	00h	-	BTCLC [1:0]			-	CLCKC[2:0]			
BT4CTR	Dir	R/W	B9h	B900h	00h	-	BTHA[1:0]			-	HCKA[2:0]			Set VGH boosting times/frequency
				B901h	00h	-	BTHB[1:0]			-	HCKB[2:0]			
				B902h	00h	-	BTHC[1:0]			-	HCKC[2:0]			
BT5CTR	Dir	R/W	BAh	BA00h	00h	-	BTLA[1:0]			-	LCKA[2:0]			Set VGLX boosting times/frequency
				BA01h	00h	-	BTLB[1:0]			-	LCKB[2:0]			
				BA02h	00h	-	BTLC[1:0]			-	LCKC[2:0]			
PFMCTR	Dir	R/W	BBh	BB00h	00h	PLIM[3:0]				NLIM[3:0]				Current limit for PFM1/2
SETVGP	Dir	R/W	BCh	BC00h	00h	-	-	-	VGMP [8]	-	-	-	VGSP [8]	Set VGMP/VGSP voltages
				BC01h	00h	VGMP[7:0]								
				BC02h	00h	VGSP[7:0]								
SETVGN	Dir	R/W	BDh	BD00h	00h	-	-	-	VGMN [8]	-	-	-	VGSN [8]	Set VGMN/VGSN voltages
				BD01h	00h	VGMN[7:0]								
				BD02h	00h	VGSN[7:0]								
SETVCMOFF	Dir	R/W	BEh	BE00h	00h	-	-	-	VCMOF FSEL	-	-	-	VCM[8]	Setting DC VCOM offset
				BE01h	00h	VCM[7:0]								
VGHCTR	Dir	R/W	BFh	BF00h	00h							VGHS[1:0]		VGH output voltage control

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDIDIC	Dir	R	C5h	C500h	00h	ID41[7:0]								Read ID4 for Chip Code (ID41~42) Chip Version (ID43)
				C501h	00h	ID42[7:0]								
				C502h	00h	-	-	-	-	ID43[3:0]				
RDIDPRD	Dir	R	C6h	C600h	00h	-	-	ID51[5:0]						Read ID5 for Lot ID(ID51~53) Wafer ID (ID54) Wafer Map (ID55~56)
				C601h	00h	-	-	ID52[5:0]						
				C602h	00h	-	-	ID53[5:0]						
				C603h	00h	-	-	-	ID54[4:0]					
				C604h	00h	-	-	-	-	-	-	ID55[9:8]		
				C605h	00h	ID55[7:0]								
				C606h	00h	-	-	-	-	ID56[3:0]				
WRDID	Dir	R/W	C7h	C700h	00h	ID1[7:0]								Write display ID code (for User Command Set DA00h~DC00h)
				C701h	00h	ID2[7:0]								
				C702h	00h	ID3[7:0]								
WRPCLRC	Dir	R/W	C8h	C800h	00h	Bkx[1:0]		Bky[1:0]		Wx[1:0]		Wy[1:0]		Write panel color characteristics (for User Command Set 7000h~7E00h)
				C801h	00h	Bkx[9:2]								
				C802h	00h	Bky[9:2]								
				C803h	00h	Wx[9:2]								
				C804h	00h	Wy[9:2]								
				C805h	00h	Rx[1:0]		Ry[1:0]		Gx[1:0]		Gy[1:0]		
				C806h	00h	Rx[9:2]								
				C807h	00h	Ry[9:2]								
				C808h	00h	Gx[9:2]								
				C809h	00h	Gy[9:2]								
				C80Ah	00h	Bx[1:0]		By[1:0]		Ax[1:0]		Ay[1:0]		
				C80Bh	00h	Bx[9:2]								
				C80Ch	00h	By[9:2]								
				C80Dh	00h	Ax[9:2]								
				C80Eh	00h	Ay[9:2]								
WRDDB	Dir	R/W	C9h	C900h	00h	SID[7:0]								Write DDB (for User Command Set A1xxh, A8xxh)
				C901h	00h	SID[15:8]								
				C902h	00h	MID[7:0]								
				C903h	00h	MID[15:8]								
GMGRDCTR	Dir	R/W	D0h	D000h	00h	-	-	-	VGP1IN[4:0]					Set gradient for gamma divider
				D001h	00h	-	-	-	VGP1OUT[4:0]					
				D002h	00h	-	-	-	VGP2IN[4:0]					
				D003h	00h	-	-	-	VGP2OUT[4:0]					

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GMRCTR1	Dir	R/W	D1h	D100h	00h	-	-	-	-	-	-	V0R1[9:8]		Set gamma 2.2 correction characteristic for positive "Red"
				D101h	00h	V0R1[7:0]								
				D102h	00h	-	-	-	-	-	-	V1R1[9:8]		
				D103h	00h	V1R1[7:0]								
				D104h	00h	-	-	-	-	-	-	V3R1[9:8]		
				D105h	00h	V3R1[7:0]								
				D106h	00h	-	-	-	-	-	-	V5R1[9:8]		
				D107h	00h	V5R1[7:0]								
				D108h	00h	-	-	-	-	-	-	V7R1[9:8]		
				D109h	00h	V7R1[7:0]								
				D10Ah	00h	-	-	-	-	-	-	V11R1[9:8]		
				D10Bh	00h	V11R1[7:0]								
				D10Ch	00h	-	-	-	-	-	-	V15R1[9:8]		
				D10Dh	00h	V15R1[7:0]								
				D10Eh	00h	-	-	-	-	-	-	V23R1[9:8]		
				D10Fh	00h	V23R1[7:0]								
				D110h	00h	-	-	-	-	-	-	V31R1[9:8]		
				D111h	00h	V31R1[7:0]								
				D112h	00h	-	-	-	-	-	-	V47R1[9:8]		
				D113h	00h	V47R1[7:0]								
				D114h	00h	-	-	-	-	-	-	V63R1[9:8]		
				D115h	00h	V63R1[7:0]								
				D116h	00h	-	-	-	-	-	-	V95R1[9:8]		
				D117h	00h	V95R1[7:0]								
				D118h	00h	-	-	-	-	-	-	V127R1[9:8]		
				D119h	00h	V127R1[7:0]								
				D11Ah	00h	-	-	-	-	-	-	V128R1[9:8]		
				D11Bh	00h	V128R1[7:0]								
				D11Ch	00h	-	-	-	-	-	-	V160R1[9:8]		
				D11Dh	00h	V160R1[7:0]								
				D11Eh	00h	-	-	-	-	-	-	V192R1[9:8]		
				D11Fh	00h	V192R1[7:0]								
				D120h	00h	-	-	-	-	-	-	V208R1[9:8]		
				D121h	00h	V208R1[7:0]								
				D122h	00h	-	-	-	-	-	-	V224R1[9:8]		
				D123h	00h	V224R1[7:0]								
				D124h	00h	-	-	-	-	-	-	V232R1[9:8]		
				D125h	00h	V232R1[7:0]								
				D126h	00h	-	-	-	-	-	-	V240R1[9:8]		
				D127h	00h	V240R1[7:0]								
				D128h	00h	-	-	-	-	-	-	V244R1[9:8]		
				D129h	00h	V244R1[7:0]								
				D12Ah	00h	-	-	-	-	-	-	V248R1[9:8]		
				D12Bh	00h	V248R1[7:0]								
				D12Ch	00h	-	-	-	-	-	-	V250R1[9:8]		
				D12Dh	00h	V250R1[7:0]								
				D12Eh	00h	-	-	-	-	-	-	V252R1[9:8]		
				D12Fh	00h	V252R1[7:0]								
				D130h	00h	-	-	-	-	-	-	V254R1[9:8]		
				D131h	00h	V254R1[7:0]								
				D132h	00h	-	-	-	-	-	-	V255R1[9:8]		
				D133h	00h	V255R1[7:0]								

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GMGCTR1	Dir	R/W	D2h	D200h	00h	-	-	-	-	-	-	V0G1[9:8]		Set gamma 2.2 correction characteristic for positive "Green"
				D201h	00h	V0G1[7:0]								
				D202h	00h	-	-	-	-	-	-	V1G1[9:8]		
				D203h	00h	V1G1[7:0]								
				D204h	00h	-	-	-	-	-	-	V3G1[9:8]		
				D205h	00h	V3G1[7:0]								
				D206h	00h	-	-	-	-	-	-	V5G1[9:8]		
				D207h	00h	V5G1[7:0]								
				D208h	00h	-	-	-	-	-	-	V7G1[9:8]		
				D209h	00h	V7G1[7:0]								
				D20Ah	00h	-	-	-	-	-	-	V11G1[9:8]		
				D20Bh	00h	V11G1[7:0]								
				D20Ch	00h	-	-	-	-	-	-	V15G1[9:8]		
				D20Dh	00h	V15G1[7:0]								
				D20Eh	00h	-	-	-	-	-	-	V23G1[9:8]		
				D20Fh	00h	V23G1[7:0]								
				D210h	00h	-	-	-	-	-	-	V31G1[9:8]		
				D211h	00h	V31G1[7:0]								
				D212h	00h	-	-	-	-	-	-	V47G1[9:8]		
				D213h	00h	V47G1[7:0]								
				D214h	00h	-	-	-	-	-	-	V63G1[9:8]		
				D215h	00h	V63G1[7:0]								
				D216h	00h	-	-	-	-	-	-	V95G1[9:8]		
				D217h	00h	V95G1[7:0]								
				D218h	00h	-	-	-	-	-	-	V127G1[9:8]		
				D219h	00h	V127G1[7:0]								
				D21Ah	00h	-	-	-	-	-	-	V128G1[9:8]		
				D21Bh	00h	V128G1[7:0]								
				D21Ch	00h	-	-	-	-	-	-	V160G1[9:8]		
				D21Dh	00h	V160G1[7:0]								
				D21Eh	00h	-	-	-	-	-	-	V192G1[9:8]		
				D21Fh	00h	V192G1[7:0]								
				D220h	00h	-	-	-	-	-	-	V208G1[9:8]		
				D221h	00h	V208G1[7:0]								
				D222h	00h	-	-	-	-	-	-	V224G1[9:8]		
				D223h	00h	V224G1[7:0]								
				D224h	00h	-	-	-	-	-	-	V232G1[9:8]		
				D225h	00h	V232G1[7:0]								
				D226h	00h	-	-	-	-	-	-	V240G1[9:8]		
				D227h	00h	V240G1[7:0]								
				D228h	00h	-	-	-	-	-	-	V244G1[9:8]		
				D229h	00h	V244G1[7:0]								
				D22Ah	00h	-	-	-	-	-	-	V248G1[9:8]		
				D22Bh	00h	V248G1[7:0]								
				D22Ch	00h	-	-	-	-	-	-	V250G1[9:8]		
				D22Dh	00h	V250G1[7:0]								
				D22Eh	00h	-	-	-	-	-	-	V252G1[9:8]		
				D22Fh	00h	V252G1[7:0]								
				D230h	00h	-	-	-	-	-	-	V254G1[9:8]		
				D231h	00h	V254G1[7:0]								
				D232h	00h	-	-	-	-	-	-	V255G1[9:8]		
				D233h	00h	V255G1[7:0]								

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GMBCTR1	Dir	R/W	D3h	D300h	00h	-	-	-	-	-	-	V0B1[9:8]		Set gamma 2.2 correction characteristic for positive "Blue"
				D301h	00h	V0B1[7:0]								
				D302h	00h	-	-	-	-	-	-	V1B1[9:8]		
				D303h	00h	V1B1[7:0]								
				D304h	00h	-	-	-	-	-	-	V3B1[9:8]		
				D305h	00h	V3B1[7:0]								
				D306h	00h	-	-	-	-	-	-	V5B1[9:8]		
				D307h	00h	V5B1[7:0]								
				D308h	00h	-	-	-	-	-	-	V7B1[9:8]		
				D309h	00h	V7B1[7:0]								
				D30Ah	00h	-	-	-	-	-	-	V11B1[9:8]		
				D30Bh	00h	V11B1[7:0]								
				D30Ch	00h	-	-	-	-	-	-	V15B1[9:8]		
				D30Dh	00h	V15B1[7:0]								
				D30Eh	00h	-	-	-	-	-	-	V23B1[9:8]		
				D30Fh	00h	V23B1[7:0]								
				D310h	00h	-	-	-	-	-	-	V31B1[9:8]		
				D311h	00h	V31B1[7:0]								
				D312h	00h	-	-	-	-	-	-	V47B1[9:8]		
				D313h	00h	V47B1[7:0]								
				D314h	00h	-	-	-	-	-	-	V63B1[9:8]		
				D315h	00h	V63B1[7:0]								
				D316h	00h	-	-	-	-	-	-	V95B1[9:8]		
				D317h	00h	V95B1[7:0]								
				D318h	00h	-	-	-	-	-	-	V127B1[9:8]		
				D319h	00h	V127B1[7:0]								
				D31Ah	00h	-	-	-	-	-	-	V128B1[9:8]		
				D31Bh	00h	V128B1[7:0]								
				D31Ch	00h	-	-	-	-	-	-	V160B1[9:8]		
				D31Dh	00h	V160B1[7:0]								
				D31Eh	00h	-	-	-	-	-	-	V192B1[9:8]		
				D31Fh	00h	V192B1[7:0]								
				D320h	00h	-	-	-	-	-	-	V208B1[9:8]		
				D321h	00h	V208B1[7:0]								
				D322h	00h	-	-	-	-	-	-	V224B1[9:8]		
				D323h	00h	V224B1[7:0]								
				D324h	00h	-	-	-	-	-	-	V232B1[9:8]		
				D325h	00h	V232B1[7:0]								
				D326h	00h	-	-	-	-	-	-	V240B1[9:8]		
				D327h	00h	V240B1[7:0]								
				D328h	00h	-	-	-	-	-	-	V244B1[9:8]		
				D329h	00h	V244B1[7:0]								
				D32Ah	00h	-	-	-	-	-	-	V248B1[9:8]		
				D32Bh	00h	V248B1[7:0]								
				D32Ch	00h	-	-	-	-	-	-	V250B1[9:8]		
				D32Dh	00h	V250B1[7:0]								
				D32Eh	00h	-	-	-	-	-	-	V252B1[9:8]		
				D32Fh	00h	V252B1[7:0]								
				D330h	00h	-	-	-	-	-	-	V254B1[9:8]		
				D331h	00h	V254B1[7:0]								
				D332h	00h	-	-	-	-	-	-	V255B1[9:8]		
				D333h	00h	V255B1[7:0]								

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GMRCTR2	Dir	R/W	D4h	D400h	00h	-	-	-	-	-	-	V0R2[9:8]		Set gamma 2.2 correction characteristic for negative "Red"
				D401h	00h	V0R2[7:0]								
				D402h	00h	-	-	-	-	-	-	V1R2[9:8]		
				D403h	00h	V1R2[7:0]								
				D404h	00h	-	-	-	-	-	-	V3R2[9:8]		
				D405h	00h	V3R2[7:0]								
				D406h	00h	-	-	-	-	-	-	V5R2[9:8]		
				D407h	00h	V5R2[7:0]								
				D408h	00h	-	-	-	-	-	-	V7R2[9:8]		
				D409h	00h	V7R2[7:0]								
				D40Ah	00h	-	-	-	-	-	-	V11R2[9:8]		
				D40Bh	00h	V11R2[7:0]								
				D40Ch	00h	-	-	-	-	-	-	V15R2[9:8]		
				D40Dh	00h	V15R2[7:0]								
				D40Eh	00h	-	-	-	-	-	-	V23R2[9:8]		
				D40Fh	00h	V23R2[7:0]								
				D410h	00h	-	-	-	-	-	-	V31R2[9:8]		
				D411h	00h	V31R2[7:0]								
				D412h	00h	-	-	-	-	-	-	V47R2[9:8]		
				D413h	00h	V47R2[7:0]								
				D414h	00h	-	-	-	-	-	-	V63R2[9:8]		
				D415h	00h	V63R2[7:0]								
				D416h	00h	-	-	-	-	-	-	V95R2[9:8]		
				D417h	00h	V95R2[7:0]								
				D418h	00h	-	-	-	-	-	-	V127R2[9:8]		
				D419h	00h	V127R2[7:0]								
				D41Ah	00h	-	-	-	-	-	-	V128R2[9:8]		
				D41Bh	00h	V128R2[7:0]								
				D41Ch	00h	-	-	-	-	-	-	V160R2[9:8]		
				D41Dh	00h	V160R2[7:0]								
				D41Eh	00h	-	-	-	-	-	-	V192R2[9:8]		
				D41Fh	00h	V192R2[7:0]								
				D420h	00h	-	-	-	-	-	-	V208R2[9:8]		
				D421h	00h	V208R2[7:0]								
				D422h	00h	-	-	-	-	-	-	V224R2[9:8]		
				D423h	00h	V224R2[7:0]								
				D424h	00h	-	-	-	-	-	-	V232R2[9:8]		
				D425h	00h	V232R2[7:0]								
				D426h	00h	-	-	-	-	-	-	V240R2[9:8]		
				D427h	00h	V240R2[7:0]								
				D428h	00h	-	-	-	-	-	-	V244R2[9:8]		
				D429h	00h	V244R2[7:0]								
				D42Ah	00h	-	-	-	-	-	-	V248R2[9:8]		
				D42Bh	00h	V248R2[7:0]								
				D42Ch	00h	-	-	-	-	-	-	V250R2[9:8]		
				D42Dh	00h	V250R2[7:0]								
				D42Eh	00h	-	-	-	-	-	-	V252R2[9:8]		
				D42Fh	00h	V252R2[7:0]								
				D430h	00h	-	-	-	-	-	-	V254R2[9:8]		
				D431h	00h	V254R2[7:0]								
				D432h	00h	-	-	-	-	-	-	V255R2[9:8]		
				D433h	00h	V255R2[7:0]								

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GMGCTR2	Dir	R/W	D5h	D500h	00h	-	-	-	-	-	-	V0G2[9:8]		Set gamma 2.2 correction characteristic for negative "Green"
				D501h	00h	V0G2[7:0]								
				D502h	00h	-	-	-	-	-	-	V1G2[9:8]		
				D503h	00h	V1G2[7:0]								
				D504h	00h	-	-	-	-	-	-	V3G2[9:8]		
				D505h	00h	V3G2[7:0]								
				D506h	00h	-	-	-	-	-	-	V5G2[9:8]		
				D507h	00h	V5G2[7:0]								
				D508h	00h	-	-	-	-	-	-	V7G2[9:8]		
				D509h	00h	V7G2[7:0]								
				D50Ah	00h	-	-	-	-	-	-	V11G2[9:8]		
				D50Bh	00h	V11G2[7:0]								
				D50Ch	00h	-	-	-	-	-	-	V15G2[9:8]		
				D50Dh	00h	V15G2[7:0]								
				D50Eh	00h	-	-	-	-	-	-	V23G2[9:8]		
				D50Fh	00h	V23G2[7:0]								
				D510h	00h	-	-	-	-	-	-	V31G2[9:8]		
				D511h	00h	V31G2[7:0]								
				D512h	00h	-	-	-	-	-	-	V47G2[9:8]		
				D513h	00h	V47G2[7:0]								
				D514h	00h	-	-	-	-	-	-	V63G2[9:8]		
				D515h	00h	V63G2[7:0]								
				D516h	00h	-	-	-	-	-	-	V95G2[9:8]		
				D517h	00h	V95G2[7:0]								
				D518h	00h	-	-	-	-	-	-	V127G2[9:8]		
				D519h	00h	V127G2[7:0]								
				D51Ah	00h	-	-	-	-	-	-	V128G2[9:8]		
				D51Bh	00h	V128G2[7:0]								
				D51Ch	00h	-	-	-	-	-	-	V160G2[9:8]		
				D51Dh	00h	V160G2[7:0]								
				D51Eh	00h	-	-	-	-	-	-	V192G2[9:8]		
				D51Fh	00h	V192G2[7:0]								
				D520h	00h	-	-	-	-	-	-	V208G2[9:8]		
				D521h	00h	V208G2[7:0]								
				D522h	00h	-	-	-	-	-	-	V224G2[9:8]		
				D523h	00h	V224G2[7:0]								
				D524h	00h	-	-	-	-	-	-	V232G2[9:8]		
				D525h	00h	V232G2[7:0]								
				D526h	00h	-	-	-	-	-	-	V240G2[9:8]		
				D527h	00h	V240G2[7:0]								
				D528h	00h	-	-	-	-	-	-	V244G2[9:8]		
				D529h	00h	V244G2[7:0]								
				D52Ah	00h	-	-	-	-	-	-	V248G2[9:8]		
				D52Bh	00h	V248G2[7:0]								
				D52Ch	00h	-	-	-	-	-	-	V250G2[9:8]		
				D52Dh	00h	V250G2[7:0]								
				D52Eh	00h	-	-	-	-	-	-	V252G2[9:8]		
				D52Fh	00h	V252G2[7:0]								
				D530h	00h	-	-	-	-	-	-	V254G2[9:8]		
				D531h	00h	V254G2[7:0]								
				D532h	00h	-	-	-	-	-	-	V255G2[9:8]		
				D533h	00h	V255G2[7:0]								

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GMBCTR2	Dir	R/W	D6h	D600h	00h	-	-	-	-	-	-	V0B2[9:8]		Set gamma 2.2 correction characteristic for negative "Blue"
				D601h	00h	V0B2[7:0]								
				D602h	00h	-	-	-	-	-	-	V1B2[9:8]		
				D603h	00h	V1B2[7:0]								
				D604h	00h	-	-	-	-	-	-	V3B2[9:8]		
				D605h	00h	V3B2[7:0]								
				D606h	00h	-	-	-	-	-	-	V5B2[9:8]		
				D607h	00h	V5B2[7:0]								
				D608h	00h	-	-	-	-	-	-	V7B2[9:8]		
				D609h	00h	V7B2[7:0]								
				D60Ah	00h	-	-	-	-	-	-	V11B2[9:8]		
				D60Bh	00h	V11B2[7:0]								
				D60Ch	00h	-	-	-	-	-	-	V15B2[9:8]		
				D60Dh	00h	V15B2[7:0]								
				D60Eh	00h	-	-	-	-	-	-	V23B2[9:8]		
				D60Fh	00h	V23B2[7:0]								
				D610h	00h	-	-	-	-	-	-	V31B2[9:8]		
				D611h	00h	V31B2[7:0]								
				D612h	00h	-	-	-	-	-	-	V47B2[9:8]		
				D613h	00h	V47B2[7:0]								
				D614h	00h	-	-	-	-	-	-	V63B2[9:8]		
				D615h	00h	V63B2[7:0]								
				D616h	00h	-	-	-	-	-	-	V95B2[9:8]		
				D617h	00h	V95B2[7:0]								
				D618h	00h	-	-	-	-	-	-	V127B2[9:8]		
				D619h	00h	V127B2[7:0]								
				D61Ah	00h	-	-	-	-	-	-	V128B2[9:8]		
				D61Bh	00h	V128B2[7:0]								
				D61Ch	00h	-	-	-	-	-	-	V160B2[9:8]		
				D61Dh	00h	V160B2[7:0]								
				D61Eh	00h	-	-	-	-	-	-	V192B2[9:8]		
				D61Fh	00h	V192B2[7:0]								
				D620h	00h	-	-	-	-	-	-	V208B2[9:8]		
				D621h	00h	V208B2[7:0]								
				D622h	00h	-	-	-	-	-	-	V224B2[9:8]		
				D623h	00h	V224B2[7:0]								
				D624h	00h	-	-	-	-	-	-	V232B2[9:8]		
				D625h	00h	V232B2[7:0]								
				D626h	00h	-	-	-	-	-	-	V240B2[9:8]		
				D627h	00h	V240B2[7:0]								
				D628h	00h	-	-	-	-	-	-	V244B2[9:8]		
				D629h	00h	V244B2[7:0]								
				D62Ah	00h	-	-	-	-	-	-	V248B2[9:8]		
				D62Bh	00h	V248B2[7:0]								
				D62Ch	00h	-	-	-	-	-	-	V250B2[9:8]		
				D62Dh	00h	V250B2[7:0]								
				D62Eh	00h	-	-	-	-	-	-	V252B2[9:8]		
				D62Fh	00h	V252B2[7:0]								
				D630h	00h	-	-	-	-	-	-	V254B2[9:8]		
				D631h	00h	V254B2[7:0]								
				D632h	00h	-	-	-	-	-	-	V255B2[9:8]		
				D633h	00h	V255B2[7:0]								

Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
MTPDET	Dir	R	ECh	EC00h	00h	-	-	-	-	-	-	-	MTP_DET	MTP power detection
MTPEN	Dir	R/W	EDh	ED00h	00h	MTP_EN1[7:0]								MTP enable
MTPWR	Dir	W	EEh	EE00h	00h	1	0	1	0	0	1	0	1	MTP write
				EE01h	00h	0	1	0	1	1	0	1	0	
				EE02h	00h	0	0	1	1	1	1	0	0	
RDMTP	Dir	R	EFh	EF00h	00h	MTP_STUS1[7:0]								Read MTP status
				EF01h	00h	MTP_STUS2[7:0]								

NOTE:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line

2. The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit SPI and 4-wire 8-bit SPI.

SETAVDD: Setting AVDD Voltage (Page 1, B000h~B002h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETAVDD	R/W	B0h	B000h	00h	-	-	-	VBPA4	VBPA3	VBPA2	VBPA1	VBPA0
			B001h	00h	-	-	-	VBPB4	VBPB3	VBPB2	VBPB1	VBPB0
			B002h	00h	-	-	-	VBPC4	VBPC3	VBPC2	VBPC1	VBPC0

NOTE: "-" Don't care

Description

This command is used to control the AVDD voltage in different display mode.

VBPA[4:0]: the step-up circuit 1 output voltage AVDD in normal / idle off mode.

VBPB[4:0]: the step-up circuit 1 output voltage AVDD in idle on mode.

VBPC[4:0]: the step-up circuit 1 output voltage AVDD in partial / idle off mode.

VBPA[4:0], VBPB[4:0], VBPC[4:0]	AVDD Voltage
00h	6.5V
01h	6.4V
02h	6.3V
:	: (0.1V/Step)
05h	6.0V
:	: (0.1V/Step)
12h	4.7V
13h	4.6V
14h	4.5V
15h~1Fh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	B000h (VBPA)	B001h (VBPB)	B002h (VBPC)
Power On Sequence	05h	05h	05h
S/W Reset	05h	05h	05h
H/W Reset	05h	05h	05h

SETAVEE: Setting AVEE Voltage (Page 1, B100h~B102h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETAVEE	R/W	B1h	B100h	00h	-	-	-	VBNA4	VBNA3	VBNA2	VBNA1	VBNA0
			B101h	00h	-	-	-	VBNB4	VBNB3	VBNB2	VBNB1	VBNB0
			B102h	00h	-	-	-	VBNC4	VBNC3	VBNC2	VBNC1	VBNC0

NOTE: "-" Don't care

Description

This command is used to control the AVEE voltage in different display mode.

VBNA[4:0]: the step-up circuit 2 output voltage AVEE in normal / idle off mode.

VBNB[4:0]: the step-up circuit 2 output voltage AVEE in idle on mode.

VBNC[4:0]: the step-up circuit 2 output voltage AVEE in partial / idle off mode.

VBNA[4:0], VBNB[4:0], VBNC[4:0]	AVEE Voltage
00h	-6.5V
01h	-6.4V
02h	-6.3V
:	: (0.1V/Step)
05h	-6.0V
:	: (0.1V/Step)
12h	-4.7V
13h	-4.6V
14h	-4.5V
15h~1Fh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	B100h (VBNA)	B101h (VBNB)	B102h (VBNC)
Power On Sequence	05h	05h	05h
S/W Reset	05h	05h	05h
H/W Reset	05h	05h	05h

SETVCL: Setting VCL Voltage (Page 1, B200h~B202h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVCL	R/W	B2h	B200h	00h	-	-	-	-	-	-	VBCLA1	VBCLA0
			B201h	00h	-	-	-	-	-	-	VBCLB1	VBCLB0
			B202h	00h	-	-	-	-	-	-	VBCLC1	VBCLC0

NOTE: "-" Don't care

Description

This command is used to control the VCL voltage in different display mode.

VBCLA[1:0]: the step-up circuit 3 output voltage VCL in normal / idle off mode.

VBCLB[1:0]: the step-up circuit 3 output voltage VCL in idle on mode.

VBCLC[1:0]: the step-up circuit 3 output voltage VCL in partial / idle off mode.

VBCLA[1:0], VBCLB[1:0], VBCLC[1:0]	VCL Voltage
00	-2.5V
01	-3.0V
10	-3.5V
11	-4.0V

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	B200h (VBCLA)	B201h (VBCLB)	B202h (VBCLC)
Power On Sequence	00h	00h	00h
S/W Reset	00h	00h	00h
H/W Reset	00h	00h	00h

SETVGH: Setting VGH Voltage (Page 1, B300h~B302h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVGH	R/W	B3h	B300h	00h	-	-	-	-	VBHA3	VBHA2	VBHA1	VBHA0
			B301h	00h	-	-	-	-	VBHB3	VBHB2	VBHB1	VBHB0
			B302h	00h	-	-	-	-	VBHC3	VBHC2	VBHC1	VBHC0

NOTE: "-" Don't care

Description

This command is used to control the VGH voltage in different display mode.

VBHA[3:0]: the step-up circuit 4 output voltage VGH in normal / idle off mode.

VBHB[3:0]: the step-up circuit 4 output voltage VGH in idle on mode.

VBHC[3:0]: the step-up circuit 4 output voltage VGH in partial / idle off mode.

VBHA[3:0], VBHB[3:0], VBHC[3:0]	VGH Voltage
0h	7V
1h	8V
2h	9V
:	: (1V/Step)
8h	15V
:	: (1V/Step)
9h	16V
Ah	17V
Bh	18V
Ch~Fh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	B300h (VBHA)	B301h (VBHB)	B302h (VBHC)
Power On Sequence	08h	08h	08h
S/W Reset	08h	08h	08h
H/W Reset	08h	08h	08h

SETVRGH Setting VRGH Voltage (Page 1, B400h~B402h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVRGH	R/W	B4h	B400h	00h	-	-	VRGHA5	VRGHA4	VRGHA3	VRGHA2	VRGHA1	VRGHA0
			B401h	00h	-	-	VRGHB5	VRGHB4	VRGHB3	VRGHB2	VRGHB1	VRGHB0
			B402h	00h	-	-	VRGHC5	VRGHC4	VRGHC3	VRGHC2	VRGHC1	VRGHC0

NOTE: "-" Don't care

Description

This command is used to control the VRGH voltage in different display mode.

VRGHA[5:0]: the regulator output voltage VRGH in normal / idle off mode.

VRGHB[5:0]: the regulator output voltage VRGH in idle on mode.

VRGHC[5:0]: the regulator output voltage VRGH in partial / idle off mode.

VRGHA[5:0], VRGHB[5:0], VRGHC[5:0]	VRGH Voltage
00h	1.0V
01h	1.1V
02h	1.2V
:	: (0.1V/Step)
28h	5.0V
:	: (0.1V/Step)
30h	5.8V
31h	5.9V
32h	6.0V
33h~3Fh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	B400h (VRGHA)	B401h (VRGHB)	B402h (VRGHC)
Power On Sequence	28h	28h	28h
S/W Reset	28h	28h	28h
H/W Reset	28h	28h	28h

SETVGL_REG: Setting VGL_REG Voltage (Page 1, B500h~B502h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVGL	R/W	B5h	B500h	00h	-	-	-	-	VBLA3	VBLA2	VBLA1	VBLA0
			B501h	00h	-	-	-	-	VBLB3	VBLB2	VBLB1	VBLB0
			B502h	00h	-	-	-	-	VBLC3	VBLC2	VBLC1	VBLC0

NOTE: "-" Don't care

Description

This command is used to control the VGL_REG voltage in different display mode.

VBLA[3:0]: the step-up circuit 5 output voltage VGL_REG in normal / idle off mode.

VBLB[3:0]: the step-up circuit 5 output voltage VGL_REG in idle on mode.

VBLC[3:0]: the step-up circuit 5 output voltage VGL_REG in partial / idle off mode.

VBLA[4:0], VBLB[4:0], VBLC[4:0]	VGL Voltage
00h	-2V
01h	-3V
02h	-4V
:	: (1V/Step)
08h	-10V
:	: (1V/Step)
0Bh	-13V
0Ch	-14V
0Dh	-15V
0Eh~0Fh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	B500h (VBLA)	B501h (VBLB)	B502h (VBLC)
Power On Sequence	08h	08h	08h
S/W Reset	08h	08h	08h
H/W Reset	08h	08h	08h

BT1CTR: BT1 Power Control for AVDD (Page 1, B600h~B602h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT1CTR	R/W	B6h	B600h	00h	-	BTPA2	BTPA1	BTPA0	-	PCKA2	PCKA1	PCKA0
			B601h	00h	-	BTPB2	BTPB1	BTPB0	-	PCKB2	PCKB1	PCKB0
			B602h	00h	-	BTPC2	BTPC1	BTPC0	-	PCKC2	PCKC1	PCKC0

NOTE: "-" Don't care

Description

This command is used to control the boosting times and booster clock frequency of step-up circuit 1 (AVDD) in different display mode.

BTPA[2:0]: the boosting times for step-up circuit 1 in normal / idle off mode.
PCKA[2:0]: the booster clock frequency for step-up circuit 1 in normal / idle off mode.

BTPB[2:0]: the boosting times for step-up circuit 1 in idle on mode.
PCKB[2:0]: the booster clock frequency for step-up circuit 1 in idle on mode..

BTPC[2:0]: the boosting times for step-up circuit 2 in partial / idle off mode.
PCKC[2:0]: the booster clock frequency for step-up circuit 1 in partial / idle off mode.

BTPA[2:0] BTPB[2:0] BTPC[2:0]	Boosting Times	PCKA[2:0] PCKB[2:0] PCKC[2:0]	Clock Frequency (Synchronized to Hsync)
0h	Disable	0h	Hsync / 32
1h	1.5 x VDDB	1h	Hsync / 16
2h	1.66 x VDDB	2h	Hsync / 8
3h	2.0 x VDDB	3h	Hsync / 4
4h	2.5 x VDDB	4h	Hsync / 2
5h	3.0 x VDDB	5h	Hsync
6h	reserved	6h	2 x Hsync
7h	reserved	7h	4 x Hsync

Note: When BTPA/B/C[2:0]="000", the boosting times is controlled by internal circuit automatically which according to the AVDD setting voltage (by command B0xxh of page 1) and VDDB input voltage.

<table>
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<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>B600h
(BTPA, PCKA)</th><th>B601h
(BTPB, PCKB)</th><th>B602h
(BTPC, PCKC)</th></tr>
<tr><td>Power On Sequence</td><td>44h</td><td>44h</td><td>44h</td></tr>
<tr><td>S/W Reset</td><td>44h</td><td>44h</td><td>44h</td></tr>
<tr><td>H/W Reset</td><td>44h</td><td>44h</td><td>44h</td></tr>
</table>
</td></tr>
</table>

BT2CTR: BT2 Power Control for AVEE (Page 1, B700h~B702h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT2CTR	R/W	B7h	B700h	00h	-	BTNA2	BTNA1	BTNA0	-	NCKA2	NCKA1	NCKA0
			B701h	00h	-	BTNB2	BTNB1	BTNB0	-	NCKB2	NCKB1	NCKB0
			B702h	00h	-	BTNC2	BTNC1	BTNC0	-	NCKC2	NCKC1	NCKC0

NOTE: "-" Don't care

Description

This command is used to control the boosting times and booster clock frequency of step-up circuit 2 (AVEE) in different display mode.

BTNA[2:0]: the boosting times for step-up circuit 2 in normal / idle off mode.
NCKA[2:0]: the booster clock frequency for step-up circuit 2 in normal / idle off mode.

BTNB[2:0]: the boosting times for step-up circuit 2 in idle on mode.
NCKB[2:0]: the booster clock frequency for step-up circuit 2 in idle on mode..

BTNC[2:0]: the boosting times for step-up circuit 2 in partial / idle off mode.
NCKC[2:0]: the booster clock frequency for step-up circuit 2 in partial / idle off mode.

BTNA[2:0] BTNB[2:0] BTNC[2:0]	Boosting Times	NCKA[2:0] NCKB[2:0] NCKC[2:0]	Clock Frequency (Synchronized to Hsync)
0h	Disable	0h	Hsync / 32
1h	-1.5 x VDDB	1h	Hsync / 16
2h	-2.0 x VDDB	2h	Hsync / 8
3h	-2.5 x VDDB	3h	Hsync / 4
4h	-3.0 x VDDB	4h	Hsync / 2
5h	reserved	5h	Hsync
6h	reserved	6h	2 x Hsync
7h	reserved	7h	4 x Hsync

Note: When BTNA/B/C[2:0]="000", the boosting times is controlled by internal circuit automatically which according to the AVEE setting voltage (by B1xxh of page 1) and VDDB input voltage.

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>B700h
(BTNA, NCKA)</th><th>B701h
(BTNB, NCKB)</th><th>B702h
(BTNC, NCKC)</th></tr>
<tr><td>Power On Sequence</td><td>34h</td><td>34h</td><td>34h</td></tr>
<tr><td>S/W Reset</td><td>34h</td><td>34h</td><td>34h</td></tr>
<tr><td>H/W Reset</td><td>34h</td><td>34h</td><td>34h</td></tr>
</table>
</td></tr>
</table>

BT3CTR: BT3 Power Control for VCL (Page 1, B800h~B802h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT3CTR	R/W	B8h	B800h	00h	-	-	BTCLA1	BTCLA0	-	CLCKA2	CLCKA1	CLCKA0
			B801h	00h	-	-	BTCLB1	BTCLB0	-	CLCKB2	CLCKB1	CLCKB0
			B802h	00h	-	-	BTCLC1	BTCLC0	-	CLCKC2	CLCKC1	CLCKC0

NOTE: "-" Don't care

Description

This command is used to control the boosting times and booster clock frequency of step-up circuit 3 (VCL) in different display mode.

BTCLA[1:0]: the boosting times for step-up circuit 3 in normal / idle off mode.
CLCKA[2:0]: the booster clock frequency for step-up circuit 3 in normal / idle off mode.

BTCLB[1:0]: the boosting times for step-up circuit 3 in idle on mode.
CLCKB[2:0]: the booster clock frequency for step-up circuit 3 in idle on mode..

BTCLC[1:0]: the boosting times for step-up circuit 3 in partial / idle off mode.
CLCKC[2:0]: the booster clock frequency for step-up circuit 3 in partial / idle off mode.

BTCLA[1:0] BTCLB[1:0] BTCLC[10]	Boosting Times
0h	Disable
1h	-0.5 x VDDB
2h	-1.0 x VDDB
3h	-2.0 x VDDB

CLCKA[2:0] CLCKB[2:0] CLCKC[2:0]	Clock Frequency (Synchronized to Hsync)
0h	Hsync / 32
1h	Hsync / 16
2h	Hsync / 8
3h	Hsync / 4
4h	Hsync / 2
5h	Hsync
6h	2 x Hsync
7h	4 x Hsync

Note: When BTCLA/B/C[2:0]="00", the boosting times is controlled by internal circuit automatically which according to the VCL setting voltage (by B2xxh of page 1) and VDDB input voltage.

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>B800h
(BTCLA, CLCKA)</th><th>B801h
(BTCLB, CLCKB)</th><th>B802h
(BTCLC, CLCKC)</th></tr>
<tr><td>Power On Sequence</td><td>24h</td><td>24h</td><td>24h</td></tr>
<tr><td>S/W Reset</td><td>24h</td><td>24h</td><td>24h</td></tr>
<tr><td>H/W Reset</td><td>24h</td><td>24h</td><td>24h</td></tr>
</table>
</td></tr>
</table>

BT4CTR: BT4 Power Control for VGH (Page 1, B900h~B902h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT4CTR	R/W	B9h	B900h	00h	-	-	BTHA1	BTHA0	-	HCKA2	HCKA1	HCKA0
			B901h	00h	-	-	BTHB1	BTHB0	-	HCKB2	HCKB1	HCKB0
			B902h	00h	-	-	BTHC1	BTHC0	-	HCKC2	HCKC1	HCKC0

NOTE: "-" Don't care

Description

This command is used to control the boosting times and booster clock frequency of step-up circuit 4 (VGH) in different display mode.

BTHA[1:0]: the boosting times for step-up circuit 4 in normal / idle off mode.
HCKA[2:0]: the booster clock frequency for step-up circuit 4 in normal / idle off mode.

BTHB[1:0]: the boosting times for step-up circuit 4 in idle on mode.
HCKB[2:0]: the booster clock frequency for step-up circuit 4 in idle on mode..

BTHC[1:0]: the boosting times for step-up circuit 4 in partial / idle off mode.
HCKC[2:0]: the booster clock frequency for step-up circuit 4 in partial / idle off mode.

BTHA[1:0] BTHB[1:0] BTHC[10]	Boosting Times	HCKA[2:0] HCKB[2:0] HCKC[2:0]	Clock Frequency (Synchronized to Hsync)
0h	AVDD+VDDB	0h	Hsync / 32
1h	AVDD-AVEE	1h	Hsync / 16
2h	AVDD-AVEE+VDDB	2h	Hsync / 8
3h	2xAVDD-AVEE	3h	Hsync / 4
		4h	Hsync / 2
		5h	Hsync
		6h	2 x Hsync
		7h	4 x Hsync

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>B900h
(BTHA, HCKA)</th><th>B901h
(BTHB, HCKB)</th><th>B902h
(BTHC, HCKC)</th></tr>
<tr><td>Power On Sequence</td><td>34h</td><td>34h</td><td>34h</td></tr>
<tr><td>S/W Reset</td><td>34h</td><td>34h</td><td>34h</td></tr>
<tr><td>H/W Reset</td><td>34h</td><td>34h</td><td>34h</td></tr>
</table>
</td></tr>
</table>

BT5CTR: BT5 Power Control for VGLX (Page 1, BA00h~BA02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT56CTR	R/W	BAh	BA00h	00h	-	-	BTLA1	BTLA0	-	LCKA2	LCKA1	LCKA0
			BA01h	00h	-	-	BTLB1	BTLB0	-	LCKB2	LCKB1	LCKB0
			BA02h	00h	-	-	BTLC1	BTLC0	-	LCKC2	LCKC1	LCKC0

NOTE: "-" Don't care

Description

This command is used to control the boosting times and booster clock frequency of step-up circuit 5 (VGLX) in different display mode.

BTLA[1:0]: the boosting times for step-up circuit 5 in normal / idle off mode.
LCKA[2:0]: the booster clock frequency for step-up circuit 5 in normal / idle off mode.

BTLB[1:0]: the boosting times for step-up circuit 5 in idle on mode.
LCKB[2:0]: the booster clock frequency for step-up circuit 5 in idle on mode..

BTLC[1:0]: the boosting times for step-up circuit 5 in partial / idle off mode.
LCKC[2:0]: the booster clock frequency for step-up circuit 5 in partial / idle off mode.

BTLA[1:0] BTLB[1:0] BTLC[10]	Boosting Times	LCKA[2:0] LCKB[2:0] LCKC[2:0]	Clock Frequency (Synchronized to Hsync)
0h	AVEE+VCL	0h	Hsync / 32
1h	AVEE-AVDD	1h	Hsync / 16
2h	AVEE+VCL-AVDD	2h	Hsync / 8
3h	2xAVEE-AVDD	3h	Hsync / 4
		4h	Hsync / 2
		5h	Hsync
		6h	2 x Hsync
		7h	4 x Hsync

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>BA00h
(BTLA, LCKA)</th><th>BA01h
(BTLB, LCKB)</th><th>BA02h
(BTLC, LCKC)</th></tr>
<tr><td>Power On Sequence</td><td>24h</td><td>24h</td><td>24h</td></tr>
<tr><td>S/W Reset</td><td>24h</td><td>24h</td><td>24h</td></tr>
<tr><td>H/W Reset</td><td>24h</td><td>24h</td><td>24h</td></tr>
</table>
</td></tr>
</table>

PFMCTR: Current Limit Control for PFM DC/DC Converter (Page 1, BB00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PFMCTR	R/W	BBh	BB00h	00h	PLIM3	PLIM2	PLIM1	PLIM0	NLIM3	NLIM2	NLIM1	NLIM0

NOTE: "-" Don't care

Description

This command is used to set the current limit for PFM1 (AVDD) and PFM2 (AVEE) respectively.

PLIM[3:0]: the current limitation control for PFM1 (AVDD) circuits.
NLIM[2:0]: the current limitation control for PFM2 (AVEED) circuits.
The limited current is decided by below formula, where limited voltage is set by PLIM[3:0]/NLIM[3:0] as below table and the external resistor is connected between CSP/CSN and Ground.

$$\text{Limited Current} = \frac{\text{Limited Voltage (mV)}}{\text{External Resistor (ohm)}}$$

PLIM[3:0]	Limited Voltage for AVDD	NLIM[3:0]	Limited Voltage for AVEE
0000	20mV	0000	20mV
0001	40mV	0001	40mV
0010	60mV	0010	60mV
0011	80mV	0011	80mV
0100	100mV	0100	100mV
0101	120mV	0101	120mV
0110	140mV	0110	140mV
0111	160mV	0111	160mV
1000	180mV	1000	180mV
1001	200mV	1001	200mV
1010	220mV	1010	220mV
1011	240mV	1011	240mV
1100	260mV	1100	260mV
1101	280mV	1101	280mV
1110	300mV	1110	300mV
1111	320mV	1111	320mV

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>BB00h (PLIM, NLIM)</th></tr>
<tr><td>Power On Sequence</td><td>44h</td></tr>
<tr><td>S/W Reset</td><td>44h</td></tr>
<tr><td>H/W Reset</td><td>44h</td></tr>
</table>
</td></tr>
</table>

SETVGP: Setting VGMP and VGSP Voltage (Page 1, BC00h~BC02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVGP	R/W	BCh	BC00h	00h	-	-	-	VGMP8	-	-	-	VGSP8
			BC01h	00h	VGMP7	VGMP6	VGMP5	VGMP4	VGMP3	VGMP2	VGMP1	VGMP0
			BC02h	00h	VGSP7	VGSP6	VGSP5	VGSP4	VGSP3	VGSP2	VGSP1	VGSP0

NOTE: "-" Don't care

Description

This command is used to set the regulator output voltage VGMP/VGSP for positive gamma divider.

VGMP1[7:0]: the high voltage for positive gamma divider.
VGSP[7:0]: the low voltage for positive gamma divider.

VGMP[8:0]	VGMP Voltage	VGSP[8:0]	VGSP Voltage
000h	3.0000V	00h	0V (GND)
001h	3.0125V	01h	0.30000V
002h	3.0250V	02h	0.30125V
:	: (12.5mV/Step)	:	:
C8h	5.5000V	:	: (12.5mV/Step)
:	: (12.5mV/Step)	:	:
106h	6.2750V	10Eh	3.6750V
107h	6.2875V	10Fh	3.6875V
108h	6.3000V	110h	3.7000V
109h~1FFh	reserved	111h~1FFh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BC00h	BC01h (VGMP)	BC02h (VGSP)
Power On Sequence	00h	C8h	00h
S/W Reset	00h	C8h	00h
H/W Reset	00h	C8h	00h

SETVGN: Setting VGMN and VGSN Voltage (Page 1, BD00h~BD02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVGP	R/W	BDh	BD00h	00h	-	-	-	VGMN8	-	-	-	VGSN8
			BD01h	00h	VGMN7	VGMN6	VGMN5	VGMN4	VGMN3	VGMN2	VGMN1	VGMN0
			BD02h	00h	VGSN7	VGSN6	VGSN5	VGSN4	VGSN3	VGSN2	VGSN1	VGSN0

NOTE: "-" Don't care

Description

This command is used to set the regulator output voltage VGMP/VGSP for negative gamma divider.

VGMN[7:0]: the high voltage for negative gamma divider.
VGSN[7:0]: the low voltage for negative gamma divider.

VGMN[8:0]	VGMN Voltage	VGSN[8:0]	VGSN Voltage
000h	-3.0000V	00h	0V (GND)
001h	-3.0125V	01h	-0.30000V
002h	-3.0250V	02h	-0.30125V
:	: (12.5mV/Step)	03h	-0.30250V
C8h	-5.5000V	:	: (12.5mV/Step)
:	: (12.5mV/Step)		
106h	-6.2750V	10Eh	-3.6750V
107h	-6.2875V	10Fh	-3.6875V
108h	-6.3000V	110h	-3.7000V
109h~1FFh	reserved	111h~1FFh	reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BD00h	BD01h (VGMN)	BD02h (VGSN)
Power On Sequence	00h	C8h	00h
S/W Reset	00h	C8h	00h
H/W Reset	00h	C8h	00h

SETVCMOFF: Setting VCOM Offset Voltage (Page 1, BE00h~BE01h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SETVCMOFF	R/W	BEh	BE00h	00h	-	-	-	VCMOFFSEL	-	-		VCM8
			BE01h	00h	VCM7	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

NOTE: "-" Don't care

Description

This command is used to adjust the DC VCOM offset voltage for panel.

VCMOFFSEL: select the voltage common voltage offset mode.

VCMOFFSEL	Common Voltage Offset Mode
0	VCOM voltage offset mode
1	Gamma voltage offset mode

VCM[8:0]: the common voltage offset for panel.

VM[8:0]	VCMOFFSEL="0"	VCMOFFSEL="1"
	VCOM Output Voltage	Internal Register Offset for Gamma Voltage (VGMP[8:0], VGSP[8:0], VGMN[8:0], VGSN[8:0])
000h	0V (GND)	0
001h	-0.0125V	1
002h	-0.0250V	2
:	: (12.5mV/Step)	:
09Fh	-1.9875V	159
0A0h	-2.0000V	160
0A1h	-2.0125V	161
:	: (12.5mV/Step)	: (1/Step)
0C7h	-2.4875V	199
0C8h	-2.5000V	200
0C9h	-2.5125V	201
:	: (12.5mV/Step)	: (1/Step)
0EFh	-2.9875V	239
0F0h	-3.0000V	240
0F1h	-3.0125V	241
:	: (12.5mV/Step)	: (1/Step)
117h	-3.4875V	279
118h	-3.5000V	280
119h~1FFh	reserved	reserved

Notes:

1. When VCOM voltage offset mode is selected:

The larger adjusted VCOM offset range the larger power consumption. The most negative VCOM voltage is clamped at VCL+0.5V. Select the proper adjusted VCOM range (by setting VCL voltage) according to panel characteristics to avoid unnecessary power consumption.

2. When Gamma voltage offset mode is selected:

The VCOM voltage will be fixed at 0V (GND). The larger AVDD (for more positive VGMP) and is necessary for gamma voltage offset.

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>BE00h</th><th>BE01h (VCM)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>00h</td></tr>
</table>
</td></tr>
</table>

VGHCTR: VGH Output Voltage (Page 1, BF00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
VGHCTR	R/W	BFh	BF00h	00h	-	-	-	-	-	-	VGHS1	VGHS0

NOTE: "-" Don't care

Description

This command is used to control the output voltage for VGH booster.

VGHS[1:0]: the enable/disable control for step-up 4 circuit.

VGHS[1:0]	Step-up 4 Circuit (VGH)
00	Voltage by boost time setting
01	7 ~ 18V
1x	AVDD

Note: VGH output voltage is decided by boost time, which set by BTHA/B/C[1:0] of command BT4CTR, when VGHS[1:0]="00".

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BF00h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

RDIDIC: Read ID for IC Vender Code (Page 1, C500h~C502h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDIDIC	R	D5h	D500h	00h	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410
			D501h	00h	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420
			D502h	00h	-	-	-	-	ID433	ID432	ID431	ID430

NOTE: "-" Don't care

Description	This command returns the internal ID code. 1st and 2nd parameters: Chip ID code. "5510h" means NT35510 3rd parameter: ID43-ID40: Chip version code.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	D500h (ID41)	D501h (ID42)	D502h (ID43)
Power On Sequence	55h	10h	XXh
S/W Reset	55h	10h	XXh
H/W Reset	55h	10h	XXh

RDIDPRD: Read ID for IC Production Code (Page 1, C600h~C606h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDIDIC	R	C6h	C600h	00h	-	-	ID515	ID514	ID513	ID512	ID511	ID510
			C601h	00h	-	-	ID525	ID524	ID523	ID522	ID521	ID520
			C602h	00h	-	-	ID535	ID534	ID533	ID532	ID531	ID530
			C603h	00h	-	-	-	ID544	ID543	ID542	ID541	ID540
			C604h	00h	-	-	-	-	-	-	ID559	ID558
			C605h	00h	ID557	ID556	ID555	ID554	ID553	ID552	ID551	ID550
			C606h	00h	-	-	-	-	ID563	ID562	ID561	ID560

NOTE: "-" Don't care

Description	This command returns the internal ID code. 1st to 3rd parameters: IC Lot No. ID code (0~9, A~Z for each register). 4th parameter: Wafer ID code (0~25d). 5th and 6th parameters: Wafer Map ID code (X-axis coordinate). 7th parameter: Wafer Map ID code (Y-axis coordinate).
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	C600h (ID51)	C601h (ID52)	C602h (ID53)	C603h (ID54)	C604h C605h (ID55)	C606h (ID56)
Power On Sequence	XXh	XXh	XXh	XXh	XXh	XXh
S/W Reset	XXh	XXh	XXh	XXh	XXh	XXh
H/W Reset	XXh	XXh	XXh	XXh	XXh	XXh

WRDID: Write Display ID (Page 1, C700h~C702h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRDID	R/W	C7h	C700h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
			C701h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
			C702h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

NOTE: "-" Don't care

Description	This command is used to define the 24-bit display identification information. The 1st parameter (ID1): module's manufacturer ID. The 2nd parameter (ID27 to ID20): module/driver version ID (Parameter Range: 80h to FFh, i.e. the ID27 is always set to "1"). The 3rd parameter (ID37 to ID30): module/driver ID. *Note: The parameter ID1, ID2, ID3 correspond to read data of commands RDID1/2/3(DAh, DBh, DCh) respectively*.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	C700h (ID1)	C701h (ID2)	C702h (ID3)
Power On Sequence	00h	80h	00h
S/W Reset	00h	80h	00h
H/W Reset	00h	80h	00h

WRPCLRC: Write Panel Color Characteristics (Page 1, C800h~C80Eh)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRPCLRC	R/W	C8h	C800h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0
			C801h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2
			C802h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2
			C803h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2
			C804h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2
			C805h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0
			C806h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2
			C807h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2
			C808h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2
			C809h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2
			C80Ah	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0
			C80Bh	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2
			C80Ch	00h	By9	By8	By7	By6	By5	By4	By3	By2
			C80Dh	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2
			C80Eh	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2

NOTE: "-" Don't care

Description	This command is used to define the panel color characteristics for black, white, red, green, blue and A color. The Bkx[9:0] and Bky[9:0]: black color characteristics. The Wx[9:0] and Wy[9:0]: white color characteristics. The Rx[9:0] and Ry[9:0]: red color characteristics. The Gx[9:0] and Gy[9:0]: green color characteristics. The Bx[9:0] and By[9:0]: blue color characteristics. The Ax[9:0] and Ay[9:0]: A color characteristics. *Note: The parameters Bkx, Bky, Wx, Wy, Rx, Ry, Gx, Gy, Bx, By, Ax, Ay correspond to read data of commands 70h to 7Eh respectively*.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All are 00h
S/W Reset	All are 00h
H/W Reset	All are 00h

WRDDB: Write DDB (Page 1, C900h~C903h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRDDB	R/W	C9h	C900h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			C901h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
			C902h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			C903h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8

NOTE: "-" Don't care

Description	This command is used to define the supplier identification, display module identification and revision identification . *Note: The parameters SID and MID correspond to read data of command RDDDBS (A1h) or command RDDDBC (A8h) respectively*.
Restriction	-
Register Availability	
Default	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value	
	C900h, C901h (SID)	C902h, C903h (MID)
Power On Sequence	0000h	0000h
S/W Reset	0000h	0000h
H/W Reset	0000h	0000h

GMGRDCTR: Gradient Control for Gamma Voltage (Page 1, D000h~D003h)

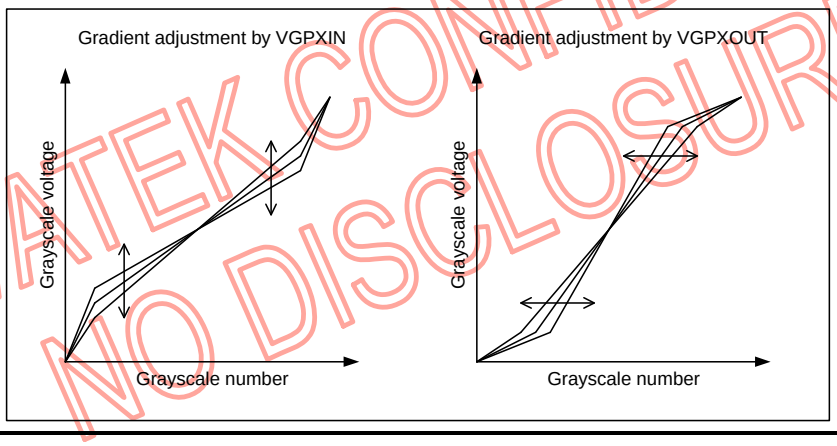
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMGRDCTR	R/W	D0h	D000h	00h	-	-	-	VGP1 IN4	VGP1 IN3	VGP1 IN2	VGP1 IN1	VGP1 IN0
			D001h	00h	-	-	-	VGP1 OUT4	VGP1 OUT3	VGP1 OUT2	VGP1 OUT1	VGP1 OUT0
			D002h	00h	-	-	-	VGP2 IN4	VGP2 IN3	VGP2 IN2	VGP2 IN1	VGP2 IN0
			D003h	00h	-	-	-	VGP2 OUT4	VGP2 OUT3	VGP2 OUT2	VGP2 OUT1	VGP2 OUT0

NOTE: "-" Don't care

Description

This command is used to set the gradient for gamma reference voltage divider.

VGP1IN[5:0] and VGP1OUT[5:0]: adjust gradient for the point close to gamma high voltage.
VGP2IN[5:0] and VGP2OUT[5:0]: adjust gradient for the point close to gamma low voltage.



Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	D000h, D001h (VGP1IN)	D002h, D003h (VGP1OUT)	D004h, D005h (VGP2IN)	D006h, D007h (VGP2OUT)
Power On Sequence	0Fh	0Fh	10h	10h
S/W Reset	0Fh	0Fh	10h	10h
H/W Reset	0Fh	0Fh	10h	10h

GMRCTR1: Setting Gamma 2.2 Correction for Red (Positive) (Page 1, D100h~D133h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMRCTR1	R/W	D1h	D100h	00h	-	-	-	-	-	-	V0R19	V0R18
			D101h	00h	V0R17	V0R16	V0R15	V0R14	V0R13	V0R12	V0R11	V0R10
			D102h	00h	-	-	-	-	-	-	V1R19	V1R18
			D103h	00h	V1R17	V1R16	V1R15	V1R14	V1R13	V1R12	V1R11	V1R10
			D104h	00h	-	-	-	-	-	-	V3R19	V3R18
			D105h	00h	V3R17	V3R16	V3R15	V3R14	V3R13	V3R12	V3R11	V3R10
			D106h	00h	-	-	-	-	-	-	V5R19	V5R18
			D107h	00h	V5R17	V5R16	V5R15	V5R14	V5R13	V5R12	V5R11	V5R10
			D108h	00h	-	-	-	-	-	-	V7R19	V7R18
			D109h	00h	V7R17	V7R16	V7R15	V7R14	V7R13	V7R12	V7R11	V7R10
			D10Ah	00h	-	-	-	-	-	-	V11R19	V11R18
			D10Bh	00h	V11R17	V11R16	V11R15	V11R14	V11R13	V11R12	V11R11	V11R10
			D10Ch	00h	-	-	-	-	-	-	V15R19	V15R18
			D10Dh	00h	V15R17	V15R16	V15R15	V15R14	V15R13	V15R12	V15R11	V15R10
			D10Eh	00h	-	-	-	-	-	-	V23R19	V23R18
			D10Fh	00h	V23R17	V23R16	V23R15	V23R14	V23R13	V23R12	V23R11	V23R10
			D110h	00h	-	-	-	-	-	-	V31R19	V31R18
			D111h	00h	V31R17	V31R16	V31R15	V31R14	V31R13	V31R12	V31R11	V31R10
			D112h	00h	-	-	-	-	-	-	V47R19	V47R18
			D113h	00h	V47R17	V47R16	V47R15	V47R14	V47R13	V47R12	V47R11	V47R10
			D114h	00h	-	-	-	-	-	-	V63R19	V63R18
			D115h	00h	V63R17	V63R16	V63R15	V63R14	V63R13	V63R12	V63R11	V63R10
			D116h	00h	-	-	-	-	-	-	V95R19	V95R18
			D117h	00h	V95R17	V95R16	V95R15	V95R14	V95R13	V95R12	V95R11	V95R10
			D118h	00h	-	-	-	-	-	-	V127 R19	V127 R18
			D119h	00h	V127 R17	V127 R16	V127 R15	V127 R14	V127 R13	V127 R12	V127 R11	V127 R10
			D11Ah	00h	-	-	-	-	-	-	V128 R19	V128 R18
			D11Bh	00h	V128 R17	V128 R16	V128 R15	V128 R14	V128 R13	V128 R12	V128 R11	V128 R10
			D11Ch	00h	-	-	-	-	-	-	V160 R19	V160 R18
			D11Dh	00h	V160 R17	V160 R16	V160 R15	V160 R14	V160 R13	V160 R12	V160 R11	V160 R10
			D11Eh	00h	-	-	-	-	-	-	V192 R19	V192 R18
			D11Fh	00h	V192 R17	V192 R16	V192 R15	V192 R14	V192 R13	V192 R12	V192 R11	V192 R10

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMRCTR1	R/W	D1h	D120h	00h	-	-	-	-	-	-	V208 R19	V208 R18
			D121h	00h	V208 R17	V208 R16	V208 R15	V208 R14	V208 R13	V208 R12	V208 R11	V208 R10
			D122h	00h	-	-	-	-	-	-	V224 R19	V224 R18
			D123h	00h	V224 R17	V224 R16	V224 R15	V224 R14	V224 R13	V224 R12	V224 R11	V224 R10
			D124h	00h	-	-	-	-	-	-	V232 R19	V232 R18
			D125h	00h	V232 R17	V232 R16	V232 R15	V232 R14	V232 R13	V232 R12	V232 R11	V232 R10
			D126h	00h	-	-	-	-	-	-	V240 R19	V240 R18
			D127h	00h	V240 R17	V240 R16	V240 R15	V240 R14	V240 R13	V240 R12	V240 R11	V240 R10
			D128h	00h	-	-	-	-	-	-	V244 R19	V244 R18
			D129h	00h	V244 R17	V244 R16	V244 R15	V244 R14	V244 R13	V244 R12	V244 R11	V244 R10
			D12Ah	00h	-	-	-	-	-	-	V248 R19	V248 R18
			D12Bh	00h	V248 R17	V248 R16	V248 R15	V248 R14	V248 R13	V248 R12	V248 R11	V248 R10
			D12Ch	00h	-	-	-	-	-	-	V250 R19	V250 R18
			D12Dh	00h	V250 R17	V250 R16	V250 R15	V250 R14	V250 R13	V250 R12	V250 R11	V250 R10
			D12Eh	00h	-	-	-	-	-	-	V252 R19	V252 R18
			D12Fh	00h	V252 R17	V252 R16	V252 R15	V252 R14	V252 R13	V252 R12	V252 R11	V252 R10
			D130h	00h	-	-	-	-	-	-	V254 R19	V254 R18
			D131h	00h	V254 R17	V254 R16	V254 R15	V254 R14	V254 R13	V254 R12	V254 R11	V254 R10
			D132h	00h	-	-	-	-	-	-	V255 R19	V255 R18
			D133h	00h	V255 R17	V255 R16	V255 R15	V255 R14	V255 R13	V255 R12	V255 R11	V255 R10

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to adjust the gamma 2.2 correction for the red (positive).

VnR1[9:0]: gamma voltage Vn for gamma 2.2 correction of red data (positive).</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>
<table>
<tr><td>D100h, D101h (V0R1)</td><td>00h, 37h</td></tr>
<tr><td>D102h, D103h (V1R1)</td><td>00h, 61h</td></tr>
<tr><td>D104h, D105h (V3R1)</td><td>00h, 92h</td></tr>
<tr><td>D106h, D107h (V5R1)</td><td>00h, B4h</td></tr>
<tr><td>D108h, D109h (V7R1)</td><td>00h, CEh</td></tr>
<tr><td>D10Ah, D10Bh (V11R1)</td><td>00h, F6h</td></tr>
<tr><td>D10Ch, D10Dh (V15R1)</td><td>01h, 14h</td></tr>
<tr><td>D10Eh, D10Fh (V23R1)</td><td>01h, 48h</td></tr>
<tr><td>D110h, D111h (V31R1)</td><td>01h, 6Bh</td></tr>
<tr><td>D112h, D113h (V47R1)</td><td>01h, A7h</td></tr>
<tr><td>D114h, D115h (V63R1)</td><td>01h, D3h</td></tr>
<tr><td>D116h, D117h (V95R1)</td><td>02h, 18h</td></tr>
<tr><td>D118h, D119h (V127R1)</td><td>02h, 50h</td></tr>
<tr><td>D11Ah, D11Bh (V128R1)</td><td>02h, 52h</td></tr>
<tr><td>D11Ch, D11Dh (V160R1)</td><td>02h, 87h</td></tr>
<tr><td>D11Eh, D11Fh (V192R1)</td><td>02h, BEh</td></tr>
<tr><td>D120h, D121h (V208R1)</td><td>02h, E2h</td></tr>
<tr><td>D122h, D123h (V224R1)</td><td>03h, 0Fh</td></tr>
<tr><td>D124h, D125h (V232R1)</td><td>03h, 30h</td></tr>
<tr><td>D126h, D127h (V240R1)</td><td>03h, 5Ch</td></tr>
<tr><td>D128h, D129h (V244R1)</td><td>03h, 77h</td></tr>
<tr><td>D12Ah, D12Bh (V248R1)</td><td>03h, 94h</td></tr>
<tr><td>D12Ch, D12Dh (V250R1)</td><td>03h, 9Fh</td></tr>
<tr><td>D12Eh, D12Fh (V252R1)</td><td>03h, ACh</td></tr>
<tr><td>D130h, D131h (V254R1)</td><td>03h, BAh</td></tr>
<tr><td>D132h, D133h (V255R1)</td><td>03h, C1h</td></tr>
</table>
</td></tr>
<tr><td>S/W Reset</td><td>Same above</td></tr>
<tr><td>H/W Reset</td><td>Same above</td></tr>
</table>
</td></tr>
</table>

GMGCTR1: Setting Gamma 2.2 Correction for Green (Positive) (Page 1, D200h~D233h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMGCTR1	R/W	D2h	D200h	00h	-	-	-	-	-	-	V0G19	V0G18
			D201h	00h	V0G17	V0G16	V0G15	V0G14	V0G13	V0G12	V0G11	V0G10
			D202h	00h	-	-	-	-	-	-	V1G19	V1G18
			D203h	00h	V1G17	V1G16	V1G15	V1G14	V1G13	V1G12	V1G11	V1G10
			D204h	00h	-	-	-	-	-	-	V3G19	V3G18
			D205h	00h	V3G17	V3G16	V3G15	V3G14	V3G13	V3G12	V3G11	V3G10
			D206h	00h	-	-	-	-	-	-	V5G19	V5G18
			D207h	00h	V5G17	V5G16	V5G15	V5G14	V5G13	V5G12	V5G11	V5G10
			D208h	00h	-	-	-	-	-	-	V7G19	V7G18
			D209h	00h	V7G17	V7G16	V7G15	V7G14	V7G13	V7G12	V7G11	V7G10
			D20Ah	00h	-	-	-	-	-	-	V11G19	V11G18
			D20Bh	00h	V11G17	V11G16	V11G15	V11G14	V11G13	V11G12	V11G11	V11G10
			D20Ch	00h	-	-	-	-	-	-	V15G19	V15G18
			D20Dh	00h	V15G17	V15G16	V15G15	V15G14	V15G13	V15G12	V15G11	V15G10
			D20Eh	00h	-	-	-	-	-	-	V23G19	V23G18
			D20Fh	00h	V23G17	V23G16	V23G15	V23G14	V23G13	V23G12	V23G11	V23G10
			D210h	00h	-	-	-	-	-	-	V31G19	V31G18
			D211h	00h	V31G17	V31G16	V31G15	V31G14	V31G13	V31G12	V31G11	V31G10
			D212h	00h	-	-	-	-	-	-	V47G19	V47G18
			D213h	00h	V47G17	V47G16	V47G15	V47G14	V47G13	V47G12	V47G11	V47G10
			D214h	00h	-	-	-	-	-	-	V63G19	V63G18
			D215h	00h	V63G17	V63G16	V63G15	V63G14	V63G13	V63G12	V63G11	V63G10
			D216h	00h	-	-	-	-	-	-	V95G19	V95G18
			D217h	00h	V95G17	V95G16	V95G15	V95G14	V95G13	V95G12	V95G11	V95G10
			D218h	00h	-	-	-	-	-	-	V127 G19	V127 G18
			D219h	00h	V127 G17	V127 G16	V127 G15	V127 G14	V127 G13	V127 G12	V127 G11	V127 G10
			D21Ah	00h	-	-	-	-	-	-	V128 G19	V128 G18
			D21Bh	00h	V128 G17	V128 G16	V128 G15	V128 G14	V128 G13	V128 G12	V128 G11	V128 G10
			D21Ch	00h	-	-	-	-	-	-	V160 G19	V160 G18
			D21Dh	00h	V160 G17	V160 G16	V160 G15	V160 G14	V160 G13	V160 G12	V160 G11	V160 G10
			D21Eh	00h	-	-	-	-	-	-	V192 G19	V192 G18
			D21Fh	00h	V192 G17	V192 G16	V192 G15	V192 G14	V192 G13	V192 G12	V192 G11	V192 G10

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMGCTR1	R/W	D2h	D220h	00h	-	-	-	-	-	-	V208 G19	V208 G18
			D221h	00h	V208 G17	V208 G16	V208 G15	V208 G14	V208 G13	V208 G12	V208 G11	V208 G10
			D222h	00h	-	-	-	-	-	-	V224 G19	V224 G18
			D223h	00h	V224 G17	V224 G16	V224 G15	V224 G14	V224 G13	V224 G12	V224 G11	V224 G10
			D224h	00h	-	-	-	-	-	-	V232 G19	V232 G18
			D225h	00h	V232 G17	V232 G16	V232 G15	V232 G14	V232 G13	V232 G12	V232 G11	V232 G10
			D226h	00h	-	-	-	-	-	-	V240 G19	V240 G18
			D227h	00h	V240 G17	V240 G16	V240 G15	V240 G14	V240 G13	V240 G12	V240 G11	V240 G10
			D228h	00h	-	-	-	-	-	-	V244 G19	V244 G18
			D229h	00h	V244 G17	V244 G16	V244 G15	V244 G14	V244 G13	V244 G12	V244 G11	V244 G10
			D22Ah	00h	-	-	-	-	-	-	V248 G19	V248 G18
			D22Bh	00h	V248 G17	V248 G16	V248 G15	V248 G14	V248 G13	V248 G12	V248 G11	V248 G10
			D22Ch	00h	-	-	-	-	-	-	V250 G19	V250 G18
			D22Dh	00h	V250 G17	V250 G16	V250 G15	V250 G14	V250 G13	V250 G12	V250 G11	V250 G10
			D22Eh	00h	-	-	-	-	-	-	V252 G19	V252 G18
			D22Fh	00h	V252 G17	V252 G16	V252 G15	V252 G14	V252 G13	V252 G12	V252 G11	V252 G10
			D230h	00h	-	-	-	-	-	-	V254 G19	V254 G18
			D231h	00h	V254 G17	V254 G16	V254 G15	V254 G14	V254 G13	V254 G12	V254 G11	V254 G10
			D232h	00h	-	-	-	-	-	-	V255 G19	V255 G18
			D233h	00h	V255 G17	V255 G16	V255 G15	V255 G14	V255 G13	V255 G12	V255 G11	V255 G10

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to adjust the gamma 2.2 correction for the green (positive).

VnG1[9:0]: gamma voltage Vn for gamma 2.2 correction of green data (positive).</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>
<table>
<tr><td>D200h, D201h (V0G1)</td><td>00h, 37h</td></tr>
<tr><td>D202h, D203h (V1G1)</td><td>00h, 61h</td></tr>
<tr><td>D204h, D205h (V3G1)</td><td>00h, 92h</td></tr>
<tr><td>D206h, D207h (V5G1)</td><td>00h, B4h</td></tr>
<tr><td>D208h, D209h (V7G1)</td><td>00h, CEh</td></tr>
<tr><td>D20Ah, D20Bh (V11G1)</td><td>00h, F6h</td></tr>
<tr><td>D20Ch, D20Dh (V15G1)</td><td>01h, 14h</td></tr>
<tr><td>D20Eh, D20Fh (V23G1)</td><td>01h, 48h</td></tr>
<tr><td>D210h, D211h (V31G1)</td><td>01h, 6Bh</td></tr>
<tr><td>D212h, D213h (V47G1)</td><td>01h, A7h</td></tr>
<tr><td>D214h, D215h (V63G1)</td><td>01h, D3h</td></tr>
<tr><td>D216h, D217h (V95G1)</td><td>02h, 18h</td></tr>
<tr><td>D218h, D219h (V127G1)</td><td>02h, 50h</td></tr>
<tr><td>D21Ah, D21Bh (V128G1)</td><td>02h, 52h</td></tr>
<tr><td>D21Ch, D21Dh (V160G1)</td><td>02h, 87h</td></tr>
<tr><td>D21Eh, D21Fh (V192G1)</td><td>02h, BEh</td></tr>
<tr><td>D220h, D221h (V208G1)</td><td>02h, E2h</td></tr>
<tr><td>D222h, D223h (V224G1)</td><td>03h, 0Fh</td></tr>
<tr><td>D224h, D225h (V232G1)</td><td>03h, 30h</td></tr>
<tr><td>D226h, D227h (V240G1)</td><td>03h, 5Ch</td></tr>
<tr><td>D228h, D229h (V244G1)</td><td>03h, 77h</td></tr>
<tr><td>D22Ah, D22Bh (V248G1)</td><td>03h, 94h</td></tr>
<tr><td>D22Ch, D22Dh (V250G1)</td><td>03h, 9Fh</td></tr>
<tr><td>D22Eh, D22Fh (V252G1)</td><td>03h, ACh</td></tr>
<tr><td>D230h, D231h (V254G1)</td><td>03h, BAh</td></tr>
<tr><td>D232h, D233h (V255G1)</td><td>03h, C1h</td></tr>
</table>
</td></tr>
<tr><td>S/W Reset</td><td>Same above</td></tr>
<tr><td>H/W Reset</td><td>Same above</td></tr>
</table>
</td></tr>
</table>

GMBCTR1: Setting Gamma 2.2 Correction for Blue (Positive) (Page 1, D300h~D333h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMBCTR1	R/W	D3h	D300h	00h	-	-	-	-	-	-	V0B19	V0B18
			D301h	00h	V0B17	V0B16	V0B15	V0B14	V0B13	V0B12	V0B11	V0B10
			D302h	00h	-	-	-	-	-	-	V1B19	V1B18
			D303h	00h	V1B17	V1B16	V1B15	V1B14	V1B13	V1B12	V1B11	V1B10
			D304h	00h	-	-	-	-	-	-	V3B19	V3B18
			D305h	00h	V3B17	V3B16	V3B15	V3B14	V3B13	V3B12	V3B11	V3B10
			D306h	00h	-	-	-	-	-	-	V5B19	V5B18
			D307h	00h	V5B17	V5B16	V5B15	V5B14	V5B13	V5B12	V5B11	V5B10
			D308h	00h	-	-	-	-	-	-	V7B19	V7B18
			D309h	00h	V7B17	V7B16	V7B15	V7B14	V7B13	V7B12	V7B11	V7B10
			D30Ah	00h	-	-	-	-	-	-	V11B19	V11B18
			D30Bh	00h	V11B17	V11B16	V11B15	V11B14	V11B13	V11B12	V11B11	V11B10
			D30Ch	00h	-	-	-	-	-	-	V15B19	V15B18
			D30Dh	00h	V15B17	V15B16	V15B15	V15B14	V15B13	V15B12	V15B11	V15B10
			D30Eh	00h	-	-	-	-	-	-	V23B19	V23B18
			D30Fh	00h	V23B17	V23B16	V23B15	V23B14	V23B13	V23B12	V23B11	V23B10
			D310h	00h	-	-	-	-	-	-	V31B19	V31B18
			D311h	00h	V31B17	V31B16	V31B15	V31B14	V31B13	V31B12	V31B11	V31B10
			D312h	00h	-	-	-	-	-	-	V47B19	V47B18
			D313h	00h	V47B17	V47B16	V47B15	V47B14	V47B13	V47B12	V47B11	V47B10
			D314h	00h	-	-	-	-	-	-	V63B19	V63B18
			D315h	00h	V63B17	V63B16	V63B15	V63B14	V63B13	V63B12	V63B11	V63B10
			D316h	00h	-	-	-	-	-	-	V95B19	V95B18
			D317h	00h	V95B17	V95B16	V95B15	V95B14	V95B13	V95B12	V95B11	V95B10
			D318h	00h	-	-	-	-	-	-	V127 B19	V127 B18
			D319h	00h	V127 B17	V127 B16	V127 B15	V127 B14	V127 B13	V127 B12	V127 B11	V127 B10
			D31Ah	00h	-	-	-	-	-	-	V128 B19	V128 B18
			D31Bh	00h	V128 B17	V128 B16	V128 B15	V128 B14	V128 B13	V128 B12	V128 B11	V128 B10
			D31Ch	00h	-	-	-	-	-	-	V160 B19	V160 B18
			D31Dh	00h	V160 B17	V160 B16	V160 B15	V160 B14	V160 B13	V160 B12	V160 B11	V160 B10
			D31Eh	00h	-	-	-	-	-	-	V192 B19	V192 B18
			D31Fh	00h	V192 B17	V192 B16	V192 B15	V192 B14	V192 B13	V192 B12	V192 B11	V192 B10

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMBCTR1	R/W	D3h	D320h	00h	-	-	-	-	-	-	V208 B19	V208 B18
			D321h	00h	V208 B17	V208 B16	V208 B15	V208 B14	V208 B13	V208 B12	V208 B11	V208 B10
			D322h	00h	-	-	-	-	-	-	V224 B19	V224 B18
			D323h	00h	V224 B17	V224 B16	V224 B15	V224 B14	V224 B13	V224 B12	V224 B11	V224 B10
			D324h	00h	-	-	-	-	-	-	V232 B19	V232 B18
			D325h	00h	V232 B17	V232 B16	V232 B15	V232 B14	V232 B13	V232 B12	V232 B11	V232 B10
			D326h	00h	-	-	-	-	-	-	V240 B19	V240 B18
			D327h	00h	V240 B17	V240 B16	V240 B15	V240 B14	V240 B13	V240 B12	V240 B11	V240 B10
			D328h	00h	-	-	-	-	-	-	V244 B19	V244 B18
			D329h	00h	V244 B17	V244 B16	V244 B15	V244 B14	V244 B13	V244 B12	V244 B11	V244 B10
			D32Ah	00h	-	-	-	-	-	-	V248 B19	V248 B18
			D32Bh	00h	V248 B17	V248 B16	V248 B15	V248 B14	V248 B13	V248 B12	V248 B11	V248 B10
			D32Ch	00h	-	-	-	-	-	-	V250 B19	V250 B18
			D32Dh	00h	V250 B17	V250 B16	V250 B15	V250 B14	V250 B13	V250 B12	V250 B11	V250 B10
			D32Eh	00h	-	-	-	-	-	-	V252 B19	V252 B18
			D32Fh	00h	V252 B17	V252 B16	V252 B15	V252 B14	V252 B13	V252 B12	V252 B11	V252 B10
			D330h	00h	-	-	-	-	-	-	V254 B19	V254 B18
			D331h	00h	V254 B17	V254 B16	V254 B15	V254 B14	V254 B13	V254 B12	V254 B11	V254 B10
			D332h	00h	-	-	-	-	-	-	V255 B19	V255 B18
			D333h	00h	V255 B17	V255 B16	V255 B15	V255 B14	V255 B13	V255 B12	V255 B11	V255 B10

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to adjust the gamma 2.2 correction for the blue (positive).

VnB1[9:0]: gamma voltage Vn for gamma 2.2 correction of blue data (positive).</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>
<table>
<tr><td>D300h, D301h (V0B1)</td><td>00h, 37h</td></tr>
<tr><td>D302h, D303h (V1B1)</td><td>00h, 61h</td></tr>
<tr><td>D304h, D305h (V3B1)</td><td>00h, 92h</td></tr>
<tr><td>D306h, D307h (V5B1)</td><td>00h, B4h</td></tr>
<tr><td>D308h, D309h (V7B1)</td><td>00h, CEh</td></tr>
<tr><td>D30Ah, D30Bh (V11B1)</td><td>00h, F6h</td></tr>
<tr><td>D30Ch, D30Dh (V15B1)</td><td>01h, 14h</td></tr>
<tr><td>D30Eh, D30Fh (V23B1)</td><td>01h, 48h</td></tr>
<tr><td>D310h, D311h (V31B1)</td><td>01h, 6Bh</td></tr>
<tr><td>D312h, D313h (V47B1)</td><td>01h, A7h</td></tr>
<tr><td>D314h, D315h (V63B1)</td><td>01h, D3h</td></tr>
<tr><td>D316h, D317h (V95B1)</td><td>02h, 18h</td></tr>
<tr><td>D318h, D319h (V127B1)</td><td>02h, 50h</td></tr>
<tr><td>D31Ah, D31Bh (V128B1)</td><td>02h, 52h</td></tr>
<tr><td>D31Ch, D31Dh (V160B1)</td><td>02h, 87h</td></tr>
<tr><td>D31Eh, D31Fh (V192B1)</td><td>02h, BEh</td></tr>
<tr><td>D320h, D321h (V208B1)</td><td>02h, E2h</td></tr>
<tr><td>D322h, D323h (V224B1)</td><td>03h, 0Fh</td></tr>
<tr><td>D324h, D325h (V232B1)</td><td>03h, 30h</td></tr>
<tr><td>D326h, D327h (V240B1)</td><td>03h, 5Ch</td></tr>
<tr><td>D328h, D329h (V244B1)</td><td>03h, 77h</td></tr>
<tr><td>D32Ah, D32Bh (V248B1)</td><td>03h, 94h</td></tr>
<tr><td>D32Ch, D32Dh (V250B1)</td><td>03h, 9Fh</td></tr>
<tr><td>D32Eh, D32Fh (V252B1)</td><td>03h, ACh</td></tr>
<tr><td>D330h, D331h (V254B1)</td><td>03h, BAh</td></tr>
<tr><td>D332h, D333h (V255B1)</td><td>03h, C1h</td></tr>
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<tr><td>S/W Reset</td><td>Same above</td></tr>
<tr><td>H/W Reset</td><td>Same above</td></tr>
</table>
</td></tr>
</table>

GMRCTR2: Setting Gamma 2.2 Correction for Red (Negative) (Page 1, D400h~D433h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMRCTR2	R/W	D4h	D400h	00h	-	-	-	-	-	-	V0R29	V0R28
			D401h	00h	V0R27	V0R26	V0R25	V0R24	V0R23	V0R22	V0R21	V0R20
			D402h	00h	-	-	-	-	-	-	V1R29	V1R28
			D403h	00h	V1R27	V1R26	V1R25	V1R24	V1R23	V1R22	V1R21	V1R20
			D404h	00h	-	-	-	-	-	-	V3R29	V3R28
			D405h	00h	V3R27	V3R26	V3R25	V3R24	V3R23	V3R22	V3R21	V3R20
			D406h	00h	-	-	-	-	-	-	V5R29	V5R28
			D407h	00h	V5R27	V5R26	V5R25	V5R24	V5R23	V5R22	V5R21	V5R20
			D408h	00h	-	-	-	-	-	-	V7R29	V7R28
			D409h	00h	V7R27	V7R26	V7R25	V7R24	V7R23	V7R22	V7R21	V7R20
			D40Ah	00h	-	-	-	-	-	-	V11R29	V11R28
			D40Bh	00h	V11R27	V11R26	V11R25	V11R24	V11R23	V11R22	V11R21	V11R20
			D40Ch	00h	-	-	-	-	-	-	V15R29	V15R28
			D40Dh	00h	V15R27	V15R26	V15R25	V15R24	V15R23	V15R22	V15R21	V15R20
			D40Eh	00h	-	-	-	-	-	-	V23R29	V23R28
			D40Fh	00h	V23R27	V23R26	V23R25	V23R24	V23R23	V23R22	V23R21	V23R20
			D410h	00h	-	-	-	-	-	-	V31R29	V31R28
			D411h	00h	V31R27	V31R26	V31R25	V31R24	V31R23	V31R22	V31R21	V31R20
			D412h	00h	-	-	-	-	-	-	V47R29	V47R28
			D413h	00h	V47R27	V47R26	V47R25	V47R24	V47R23	V47R22	V47R21	V47R20
			D414h	00h	-	-	-	-	-	-	V63R29	V63R28
			D415h	00h	V63R27	V63R26	V63R25	V63R24	V63R23	V63R22	V63R21	V63R20
			D416h	00h	-	-	-	-	-	-	V95R29	V95R28
			D417h	00h	V95R27	V95R26	V95R25	V95R24	V95R23	V95R22	V95R21	V95R20
			D418h	00h	-	-	-	-	-	-	V127 R29	V127 R28
			D419h	00h	V127 R27	V127 R26	V127 R25	V127 R24	V127 R23	V127 R22	V127 R21	V127 R20
			D41Ah	00h	-	-	-	-	-	-	V128 R29	V128 R28
			D41Bh	00h	V128 R27	V128 R26	V128 R25	V128 R24	V128 R23	V128 R22	V128 R21	V128 R20
			D41Ch	00h	-	-	-	-	-	-	V160 R29	V160 R28
			D41Dh	00h	V160 R27	V160 R26	V160 R25	V160 R24	V160 R23	V160 R22	V160 R21	V160 R20
			D41Eh	00h	-	-	-	-	-	-	V192 R29	V192 R28
			D41Fh	00h	V192 R27	V192 R26	V192 R25	V192 R24	V192 R23	V192 R22	V192 R21	V192 R20

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMRCTR2	R/W	D4h	D420h	00h	-	-	-	-	-	-	V208 R29	V208 R28
			D421h	00h	V208 R27	V208 R26	V208 R25	V208 R24	V208 R23	V208 R22	V208 R21	V208 R20
			D422h	00h	-	-	-	-	-	-	V224 R29	V224 R28
			D423h	00h	V224 R27	V224 R26	V224 R25	V224 R24	V224 R23	V224 R22	V224 R21	V224 R20
			D424h	00h	-	-	-	-	-	-	V232 R29	V232 R28
			D425h	00h	V232 R27	V232 R26	V232 R25	V232 R24	V232 R23	V232 R22	V232 R21	V232 R20
			D426h	00h	-	-	-	-	-	-	V240 R29	V240 R28
			D427h	00h	V240 R27	V240 R26	V240 R25	V240 R24	V240 R23	V240 R22	V240 R21	V240 R20
			D428h	00h	-	-	-	-	-	-	V244 R29	V244 R28
			D429h	00h	V244 R27	V244 R26	V244 R25	V244 R24	V244 R23	V244 R22	V244 R21	V244 R20
			D42Ah	00h	-	-	-	-	-	-	V248 R29	V248 R28
			D42Bh	00h	V248 R27	V248 R26	V248 R25	V248 R24	V248 R23	V248 R22	V248 R21	V248 R20
			D42Ch	00h	-	-	-	-	-	-	V250 R29	V250 R28
			D42Dh	00h	V250 R27	V250 R26	V250 R25	V250 R24	V250 R23	V250 R22	V250 R21	V250 R20
			D42Eh	00h	-	-	-	-	-	-	V252 R29	V252 R28
			D42Fh	00h	V252 R27	V252 R26	V252 R25	V252 R24	V252 R23	V252 R22	V252 R21	V252 R20
			D430h	00h	-	-	-	-	-	-	V254 R29	V254 R28
			D431h	00h	V254 R27	V254 R26	V254 R25	V254 R24	V254 R23	V254 R22	V254 R21	V254 R20
			D432h	00h	-	-	-	-	-	-	V255 R29	V255 R28
			D433h	00h	V255 R27	V255 R26	V255 R25	V255 R24	V255 R23	V255 R22	V255 R21	V255 R20

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to adjust the gamma 2.2 correction for the red (negative).

VnR2[9:0]: gamma voltage Vn for gamma 2.2 correction of red data (negative).</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>
<table>
<tr><td>D400h, D401h (V0R2)</td><td>00h, 37h</td></tr>
<tr><td>D402h, D403h (V1R2)</td><td>00h, 61h</td></tr>
<tr><td>D404h, D405h (V3R2)</td><td>00h, 92h</td></tr>
<tr><td>D406h, D407h (V5R2)</td><td>00h, B4h</td></tr>
<tr><td>D408h, D409h (V7R2)</td><td>00h, CEh</td></tr>
<tr><td>D40Ah, D40Bh (V11R2)</td><td>00h, F6h</td></tr>
<tr><td>D40Ch, D40Dh (V15R2)</td><td>01h, 14h</td></tr>
<tr><td>D40Eh, D40Fh (V23R2)</td><td>01h, 48h</td></tr>
<tr><td>D410h, D411h (V31R2)</td><td>01h, 6Bh</td></tr>
<tr><td>D412h, D413h (V47R2)</td><td>01h, A7h</td></tr>
<tr><td>D414h, D415h (V63R2)</td><td>01h, D3h</td></tr>
<tr><td>D416h, D417h (V95R2)</td><td>02h, 18h</td></tr>
<tr><td>D418h, D419h (V127R2)</td><td>02h, 50h</td></tr>
<tr><td>D41Ah, D41Bh (V128R2)</td><td>02h, 52h</td></tr>
<tr><td>D41Ch, D41Dh (V160R2)</td><td>02h, 87h</td></tr>
<tr><td>D41Eh, D41Fh (V192R2)</td><td>02h, BEh</td></tr>
<tr><td>D420h, D421h (V208R2)</td><td>02h, E2h</td></tr>
<tr><td>D422h, D423h (V224R2)</td><td>03h, 0Fh</td></tr>
<tr><td>D424h, D425h (V232R2)</td><td>03h, 30h</td></tr>
<tr><td>D426h, D427h (V240R2)</td><td>03h, 5Ch</td></tr>
<tr><td>D428h, D429h (V244R2)</td><td>03h, 77h</td></tr>
<tr><td>D42Ah, D42Bh (V248R2)</td><td>03h, 94h</td></tr>
<tr><td>D42Ch, D42Dh (V250R2)</td><td>03h, 9Fh</td></tr>
<tr><td>D42Eh, D42Fh (V252R2)</td><td>03h, ACh</td></tr>
<tr><td>D430h, D431h (V254R2)</td><td>03h, BAh</td></tr>
<tr><td>D432h, D433h (V255R2)</td><td>03h, C1h</td></tr>
</table>
</td></tr>
<tr><td>S/W Reset</td><td>Same above</td></tr>
<tr><td>H/W Reset</td><td>Same above</td></tr>
</table>
</td></tr>
</table>

GMGCTR2: Setting Gamma 2.2 Correction for Green (Negative) (Page 1, D500h~D533h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMGCTR2	R/W	D5h	D500h	00h	-	-	-	-	-	-	V0G29	V0G28
			D501h	00h	V0G27	V0G26	V0G25	V0G24	V0G23	V0G22	V0G21	V0G20
			D502h	00h	-	-	-	-	-	-	V1G29	V1G28
			D503h	00h	V1G27	V1G26	V1G25	V1G24	V1G23	V1G22	V1G21	V1G20
			D504h	00h	-	-	-	-	-	-	V3G29	V3G28
			D505h	00h	V3G27	V3G26	V3G25	V3G24	V3G23	V3G22	V3G21	V3G20
			D506h	00h	-	-	-	-	-	-	V5G29	V5G28
			D507h	00h	V5G27	V5G26	V5G25	V5G24	V5G23	V5G22	V5G21	V5G20
			D508h	00h	-	-	-	-	-	-	V7G29	V7G28
			D509h	00h	V7G27	V7G26	V7G25	V7G24	V7G23	V7G22	V7G21	V7G20
			D50Ah	00h	-	-	-	-	-	-	V11G29	V11G28
			D50Bh	00h	V11G27	V11G26	V11G25	V11G24	V11G23	V11G22	V11G21	V11G20
			D50Ch	00h	-	-	-	-	-	-	V15G29	V15G28
			D50Dh	00h	V15G27	V15G26	V15G25	V15G24	V15G23	V15G22	V15G21	V15G20
			D50Eh	00h	-	-	-	-	-	-	V23G29	V23G28
			D50Fh	00h	V23G27	V23G26	V23G25	V23G24	V23G23	V23G22	V23G21	V23G20
			D510h	00h	-	-	-	-	-	-	V31G29	V31G28
			D511h	00h	V31G27	V31G26	V31G25	V31G24	V31G23	V31G22	V31G21	V31G20
			D512h	00h	-	-	-	-	-	-	V47G29	V47G28
			D513h	00h	V47G27	V47G26	V47G25	V47G24	V47G23	V47G22	V47G21	V47G20
			D514h	00h	-	-	-	-	-	-	V63G29	V63G28
			D515h	00h	V63G27	V63G26	V63G25	V63G24	V63G23	V63G22	V63G21	V63G20
			D516h	00h	-	-	-	-	-	-	V95G29	V95G28
			D517h	00h	V95G27	V95G26	V95G25	V95G24	V95G23	V95G22	V95G21	V95G20
			D518h	00h	-	-	-	-	-	-	V127 G29	V127 G28
			D519h	00h	V127 G27	V127 G26	V127 G25	V127 G24	V127 G23	V127 G22	V127 G21	V127 G20
			D51Ah	00h	-	-	-	-	-	-	V128 G29	V128 G28
			D51Bh	00h	V128 G27	V128 G26	V128 G25	V128 G24	V128 G23	V128 G22	V128 G21	V128 G20
			D51Ch	00h	-	-	-	-	-	-	V160 G29	V160 G28
			D51Dh	00h	V160 G27	V160 G26	V160 G25	V160 G24	V160 G23	V160 G22	V160 G21	V160 G20
			D51Eh	00h	-	-	-	-	-	-	V192 G29	V192 G28
			D51Fh	00h	V192 G27	V192 G26	V192 G25	V192 G24	V192 G23	V192 G22	V192 G21	V192 G20

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMGCTR2	R/W	D5h	D520h	00h	-	-	-	-	-	-	V208 G29	V208 G28
			D521h	00h	V208 G27	V208 G26	V208 G25	V208 G24	V208 G23	V208 G22	V208 G21	V208 G20
			D522h	00h	-	-	-	-	-	-	V224 G29	V224 G28
			D523h	00h	V224 G27	V224 G26	V224 G25	V224 G24	V224 G23	V224 G22	V224 G21	V224 G20
			D524h	00h	-	-	-	-	-	-	V232 G29	V232 G28
			D525h	00h	V232 G27	V232 G26	V232 G25	V232 G24	V232 G23	V232 G22	V232 G21	V232 G20
			D526h	00h	-	-	-	-	-	-	V240 G29	V240 G28
			D527h	00h	V240 G27	V240 G26	V240 G25	V240 G24	V240 G23	V240 G22	V240 G21	V240 G20
			D528h	00h	-	-	-	-	-	-	V244 G29	V244 G28
			D529h	00h	V244 G27	V244 G26	V244 G25	V244 G24	V244 G23	V244 G22	V244 G21	V244 G20
			D52Ah	00h	-	-	-	-	-	-	V248 G29	V248 G28
			D52Bh	00h	V248 G27	V248 G26	V248 G25	V248 G24	V248 G23	V248 G22	V248 G21	V248 G20
			D52Ch	00h	-	-	-	-	-	-	V250 G29	V250 G28
			D52Dh	00h	V250 G27	V250 G26	V250 G25	V250 G24	V250 G23	V250 G22	V250 G21	V250 G20
			D52Eh	00h	-	-	-	-	-	-	V252 G29	V252 G28
			D52Fh	00h	V252 G27	V252 G26	V252 G25	V252 G24	V252 G23	V252 G22	V252 G21	V252 G20
			D530h	00h	-	-	-	-	-	-	V254 G29	V254 G28
			D531h	00h	V254 G27	V254 G26	V254 G25	V254 G24	V254 G23	V254 G22	V254 G21	V254 G20
			D532h	00h	-	-	-	-	-	-	V255 G29	V255 G28
			D533h	00h	V255 G27	V255 G26	V255 G25	V255 G24	V255 G23	V255 G22	V255 G21	V255 G20

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to adjust the gamma 2.2 correction for the green (negative).

VnG2[9:0]: gamma voltage Vn for gamma 2.2 correction of green data (negative).</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>
<table>
<tr><td>D500h, D501h (V0G2)</td><td>00h, 37h</td></tr>
<tr><td>D502h, D503h (V1G2)</td><td>00h, 61h</td></tr>
<tr><td>D504h, D505h (V3G2)</td><td>00h, 92h</td></tr>
<tr><td>D506h, D507h (V5G2)</td><td>00h, B4h</td></tr>
<tr><td>D508h, D509h (V7G2)</td><td>00h, CEh</td></tr>
<tr><td>D50Ah, D50Bh (V11G2)</td><td>00h, F6h</td></tr>
<tr><td>D50Ch, D50Dh (V15G2)</td><td>01h, 14h</td></tr>
<tr><td>D50Eh, D50Fh (V23G2)</td><td>01h, 48h</td></tr>
<tr><td>D510h, D511h (V31G2)</td><td>01h, 6Bh</td></tr>
<tr><td>D512h, D513h (V47G2)</td><td>01h, A7h</td></tr>
<tr><td>D514h, D515h (V63G2)</td><td>01h, D3h</td></tr>
<tr><td>D516h, D517h (V95G2)</td><td>02h, 18h</td></tr>
<tr><td>D518h, D519h (V127G2)</td><td>02h, 50h</td></tr>
<tr><td>D51Ah, D51Bh (V128G2)</td><td>02h, 52h</td></tr>
<tr><td>D51Ch, D51Dh (V160G2)</td><td>02h, 87h</td></tr>
<tr><td>D51Eh, D51Fh (V192G2)</td><td>02h, BEh</td></tr>
<tr><td>D520h, D521h (V208G2)</td><td>02h, E2h</td></tr>
<tr><td>D522h, D523h (V224G2)</td><td>03h, 0Fh</td></tr>
<tr><td>D524h, D525h (V232G2)</td><td>03h, 30h</td></tr>
<tr><td>D526h, D527h (V240G2)</td><td>03h, 5Ch</td></tr>
<tr><td>D528h, D529h (V244G2)</td><td>03h, 77h</td></tr>
<tr><td>D52Ah, D52Bh (V248G2)</td><td>03h, 94h</td></tr>
<tr><td>D52Ch, D52Dh (V250G2)</td><td>03h, 9Fh</td></tr>
<tr><td>D52Eh, D52Fh (V252G2)</td><td>03h, ACh</td></tr>
<tr><td>D530h, D531h (V254G2)</td><td>03h, BAh</td></tr>
<tr><td>D532h, D533h (V255G2)</td><td>03h, C1h</td></tr>
</table>
</td></tr>
<tr><td>S/W Reset</td><td>Same above</td></tr>
<tr><td>H/W Reset</td><td>Same above</td></tr>
</table>
</td></tr>
</table>

GMBCTR2: Setting Gamma 2.2 Correction for Blue (Negative) (Page 1, D600h~D633h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMBCTR2	R/W	D6h	D600h	00h	-	-	-	-	-	-	V0B29	V0B28
			D601h	00h	V0B27	V0B26	V0B25	V0B24	V0B23	V0B22	V0B21	V0B20
			D602h	00h	-	-	-	-	-	-	V1B29	V1B28
			D603h	00h	V1B27	V1B26	V1B25	V1B24	V1B23	V1B22	V1B21	V1B20
			D604h	00h	-	-	-	-	-	-	V3B29	V3B28
			D605h	00h	V3B27	V3B26	V3B25	V3B24	V3B23	V3B22	V3B21	V3B20
			D606h	00h	-	-	-	-	-	-	V5B29	V5B28
			D607h	00h	V5B27	V5B26	V5B25	V5B24	V5B23	V5B22	V5B21	V5B20
			D608h	00h	-	-	-	-	-	-	V7B29	V7B28
			D609h	00h	V7B27	V7B26	V7B25	V7B24	V7B23	V7B22	V7B21	V7B20
			D60Ah	00h	-	-	-	-	-	-	V11B29	V11B28
			D60Bh	00h	V11B27	V11B26	V11B25	V11B24	V11B23	V11B22	V11B21	V11B20
			D60Ch	00h	-	-	-	-	-	-	V15B29	V15B28
			D60Dh	00h	V15B27	V15B26	V15B25	V15B24	V15B23	V15B22	V15B21	V15B20
			D60Eh	00h	-	-	-	-	-	-	V23B29	V23B28
			D60Fh	00h	V23B27	V23B26	V23B25	V23B24	V23B23	V23B22	V23B21	V23B20
			D610h	00h	-	-	-	-	-	-	V31B29	V31B28
			D611h	00h	V31B27	V31B26	V31B25	V31B24	V31B23	V31B22	V31B21	V31B20
			D612h	00h	-	-	-	-	-	-	V47B29	V47B28
			D613h	00h	V47B27	V47B26	V47B25	V47B24	V47B23	V47B22	V47B21	V47B20
			D614h	00h	-	-	-	-	-	-	V63B29	V63B28
			D615h	00h	V63B27	V63B26	V63B25	V63B24	V63B23	V63B22	V63B21	V63B20
			D616h	00h	-	-	-	-	-	-	V95B29	V95B28
			D617h	00h	V95B27	V95B26	V95B25	V95B24	V95B23	V95B22	V95B21	V95B20
			D618h	00h	-	-	-	-	-	-	V127 B29	V127 B28
			D619h	00h	V127 B27	V127 B26	V127 B25	V127 B24	V127 B23	V127 B22	V127 B21	V127 B20
			D61Ah	00h	-	-	-	-	-	-	V128 B29	V128 B28
			D61Bh	00h	V128 B27	V128 B26	V128 B25	V128 B24	V128 B23	V128 B22	V128 B21	V128 B20
			D61Ch	00h	-	-	-	-	-	-	V160 B29	V160 B28
			D61Dh	00h	V160 B27	V160 B26	V160 B25	V160 B24	V160 B23	V160 B22	V160 B21	V160 B20
			D61Eh	00h	-	-	-	-	-	-	V192 B29	V192 B28
			D61Fh	00h	V192 B27	V192 B26	V192 B25	V192 B24	V192 B23	V192 B22	V192 B21	V192 B20

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GMBCTR2	R/W	D6h	D620h	00h	-	-	-	-	-	-	V208 B29	V208 B28
			D621h	00h	V208 B27	V208 B26	V208 B25	V208 B24	V208 B23	V208 B22	V208 B21	V208 B20
			D622h	00h	-	-	-	-	-	-	V224 B29	V224 B28
			D623h	00h	V224 B27	V224 B26	V224 B25	V224 B24	V224 B23	V224 B22	V224 B21	V224 B20
			D624h	00h	-	-	-	-	-	-	V232 B29	V232 B28
			D625h	00h	V232 B27	V232 B26	V232 B25	V232 B24	V232 B23	V232 B22	V232 B21	V232 B20
			D626h	00h	-	-	-	-	-	-	V240 B29	V240 B28
			D627h	00h	V240 B27	V240 B26	V240 B25	V240 B24	V240 B23	V240 B22	V240 B21	V240 B20
			D628h	00h	-	-	-	-	-	-	V244 B29	V244 B28
			D629h	00h	V244 B27	V244 B26	V244 B25	V244 B24	V244 B23	V244 B22	V244 B21	V244 B20
			D62Ah	00h	-	-	-	-	-	-	V248 B29	V248 B28
			D62Bh	00h	V248 B27	V248 B26	V248 B25	V248 B24	V248 B23	V248 B22	V248 B21	V248 B20
			D62Ch	00h	-	-	-	-	-	-	V250 B29	V250 B28
			D62Dh	00h	V250 B27	V250 B26	V250 B25	V250 B24	V250 B23	V250 B22	V250 B21	V250 B20
			D62Eh	00h	-	-	-	-	-	-	V252 B29	V252 B28
			D62Fh	00h	V252 B27	V252 B26	V252 B25	V252 B24	V252 B23	V252 B22	V252 B21	V252 B20
			D630h	00h	-	-	-	-	-	-	V254 B29	V254 B28
			D631h	00h	V254 B27	V254 B26	V254 B25	V254 B24	V254 B23	V254 B22	V254 B21	V254 B20
			D632h	00h	-	-	-	-	-	-	V255 B29	V255 B28
			D633h	00h	V255 B27	V255 B26	V255 B25	V255 B24	V255 B23	V255 B22	V255 B21	V255 B20

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to adjust the gamma 2.2 correction for the blue (negative).

VnB2[9:0]: gamma voltage Vn for gamma 2.2 correction of blue data (negative).</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>
<table>
<tr><td>D600h, D601h (V0B2)</td><td>00h, 37h</td></tr>
<tr><td>D602h, D603h (V1B2)</td><td>00h, 61h</td></tr>
<tr><td>D604h, D605h (V3B2)</td><td>00h, 92h</td></tr>
<tr><td>D606h, D607h (V5B2)</td><td>00h, B4h</td></tr>
<tr><td>D608h, D609h (V7B2)</td><td>00h, CEh</td></tr>
<tr><td>D60Ah, D60Bh (V11B2)</td><td>00h, F6h</td></tr>
<tr><td>D60Ch, D60Dh (V15B2)</td><td>01h, 14h</td></tr>
<tr><td>D60Eh, D60Fh (V23B2)</td><td>01h, 48h</td></tr>
<tr><td>D610h, D611h (V31B2)</td><td>01h, 6Bh</td></tr>
<tr><td>D612h, D613h (V47B2)</td><td>01h, A7h</td></tr>
<tr><td>D614h, D615h (V63B2)</td><td>01h, D3h</td></tr>
<tr><td>D616h, D617h (V95B2)</td><td>02h, 18h</td></tr>
<tr><td>D618h, D619h (V127B2)</td><td>02h, 50h</td></tr>
<tr><td>D61Ah, D61Bh (V128B2)</td><td>02h, 52h</td></tr>
<tr><td>D61Ch, D61Dh (V160B2)</td><td>02h, 87h</td></tr>
<tr><td>D61Eh, D61Fh (V192B2)</td><td>02h, BEh</td></tr>
<tr><td>D620h, D621h (V208B2)</td><td>02h, E2h</td></tr>
<tr><td>D622h, D623h (V224B2)</td><td>03h, 0Fh</td></tr>
<tr><td>D624h, D625h (V232B2)</td><td>03h, 30h</td></tr>
<tr><td>D626h, D627h (V240B2)</td><td>03h, 5Ch</td></tr>
<tr><td>D628h, D629h (V244B2)</td><td>03h, 77h</td></tr>
<tr><td>D62Ah, D62Bh (V248B2)</td><td>03h, 94h</td></tr>
<tr><td>D62Ch, D62Dh (V250B2)</td><td>03h, 9Fh</td></tr>
<tr><td>D62Eh, D62Fh (V252B2)</td><td>03h, ACh</td></tr>
<tr><td>D630h, D631h (V254B2)</td><td>03h, BAh</td></tr>
<tr><td>D632h, D633h (V255B2)</td><td>03h, C1h</td></tr>
</table>
</td></tr>
<tr><td>S/W Reset</td><td>Same above</td></tr>
<tr><td>H/W Reset</td><td>Same above</td></tr>
</table>
</td></tr>
</table>

MTPDET: MTP Power Detection (Page 1, EC00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MTPDET	R	ECh	EC00h	00h	-	-	-	-	-	-	-	MTP_ DET

NOTE: "-" Don't care

Description	This command is used to check the external power for MTP programming which is ready or not. When the pad MTP_PWR is floating or connected to ground, the read out value of MTP_DET register is "0". When the external power 7.5V is connected to the pad MTP_PWR, the read our value of MTP_DET register is "1".
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

MTPEN: MTP Enable Control (Page 1, ED00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MTPEN	R/W	EDh	ED00h	00h	MTP_ EN17	MTP_ EN16	MTP_ EN15	MTP_ EN14	MTP_ EN13	MTP_ EN12	MTP_ EN11	MTP_ EN10

NOTE: "-" Don't care

Description

This command is used to enable the different group data for MTP programming respectively.

Bit	Description	Value
MTP_EN1[7]	MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Disable
		"1": Enable
MTP_EN1[6]	MTP for gamma 2.2 correction (D0xxh~D6xxh of page 1)	"0": Disable
		"1": Enable
MTP_EN1[5]	MTP for panel color and DDB (C8xxh, C9xxh of page 1)	"0": Disable
		"1": Enable
MTP_EN1[4]	Fixed to 0	-
		-
MTP_EN1[3]	Fixed to 0	-
		-
MTP_EN1[2]	Fixed to 0	-
		-
MTP_EN1[1]	Fixed to 0	-
		-
MTP_EN1[0]	Fixed to 0	-
		-

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

MTPWR: MTP Write (Page 1, EE00h~EE02h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MTPWR	W	EEh	EE00h	00h	1	0	1	0	0	1	0	1
			EE01h	00h	0	1	0	1	1	0	1	0
			EE02h	00h	0	0	1	1	1	1	0	0

NOTE: "-" Don't care

Description	This command is MTP write command. The MTP write sequence EE00h+0xA5h → EE01h+0x5Ah → EE02h+0x3Ch must be followed for MTP programming. This function is active when the sequence above is complete and the EE02 command is executed.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	EE00h	EE01h	EE02h
Power On Sequence	A5h	5Ah	3Ch
S/W Reset	A5h	5Ah	3Ch
H/W Reset	A5h	5Ah	3Ch

RDMTP: Read MTP Status (Page 1, EF00h~EF01h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDMTP	R	EFh	EF00h	00h	MTP_STUS17	MTP_STUS16	MTP_STUS15	MTP_STUS14	MTP_STUS13	MTP_STUS12	MTP_STUS11	MTP_STUS10
			EF01h	00h	MTP_STUS27	MTP_STUS26	MTP_STUS25	MTP_STUS24	MTP_STUS23	MTP_STUS22	MTP_STUS21	MTP_STUS20

NOTE: "-" Don't care

Description

This command is represent the current status which the group data shown in command ED00h is programmed or not.

Bit	Description	Value
MTP_STUS1[7]	1st time MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Not programmed
		"1": Programmed
MTP_STUS1[6]	2nd time MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Not programmed
		"1": Programmed
MTP_STUS1[5]	3rd time MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Not programmed
		"1": Programmed
MTP_STUS1[4]	4th time MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Not programmed
		"1": Programmed
MTP_STUS1[3]	Not defined	-
		-
MTP_STUS1[2]	Not defined	-
		-
MTP_STUS1[1]	1st time MTP for gamma 2.2 correction (D0xxh~D6xxh of page 1)	"0": Not programmed
		"1": Programmed
MTP_STUS1[0]	2nd time MTP for gamma 2.2 correction (D0xxh~D6xxh of page 1)	"0": Not programmed
		"1": Programmed

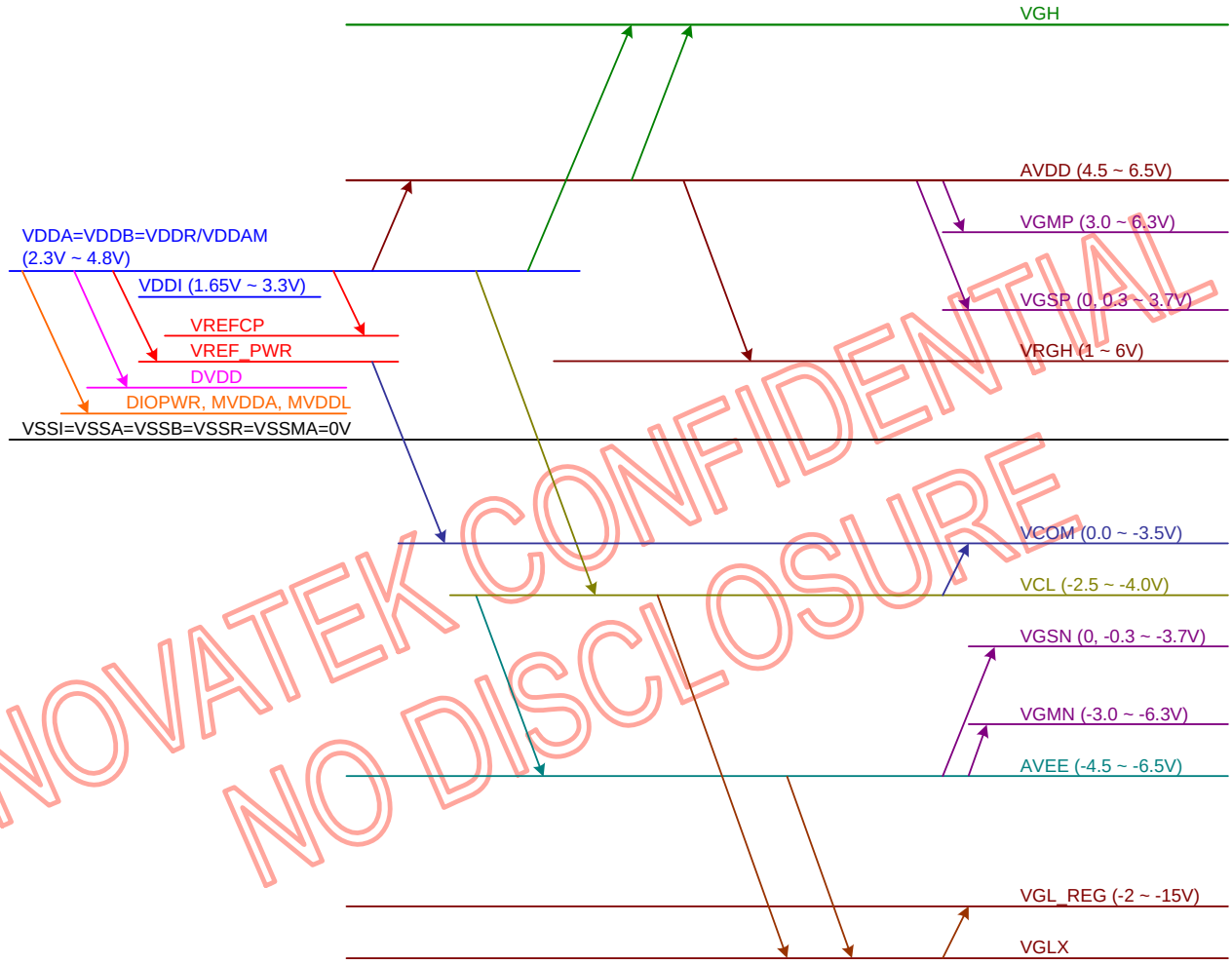
Bit	Description	Value
MTP_STUS2[7]	Not defined	-
MTP_STUS2[6]	Not defined	-
MTP_STUS2[5]	Not defined	-
MTP_STUS1[4]	1st time MTP for panel color and DDB (C8xxh, C9xxh of page 1)	"0": Not programmed
		"1": Programmed
MTP_STUS2[3]	Not defined	-
		-
MTP_STUS2[2]	Not defined	-
		-
MTP_STUS2[1]	Not defined	-
		-
MTP_STUS2[0]	Not defined	-
		-

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>MTP_STUS1</th><th>MTP_STUS2</th></tr>
<tr><td>Power On Sequence</td><td>00h (XXh after MTP)</td><td>00h (XXh after MTP)</td></tr>
<tr><td>S/W Reset</td><td>00h (XXh after MTP)</td><td>00h (XXh after MTP)</td></tr>
<tr><td>H/W Reset</td><td>00h (XXh after MTP)</td><td>00h (XXh after MTP)</td></tr>
</table>
</td></tr>
</table>

2 POWER GENERATION CIRCUIT

2.1 LCD Power Generation Scheme

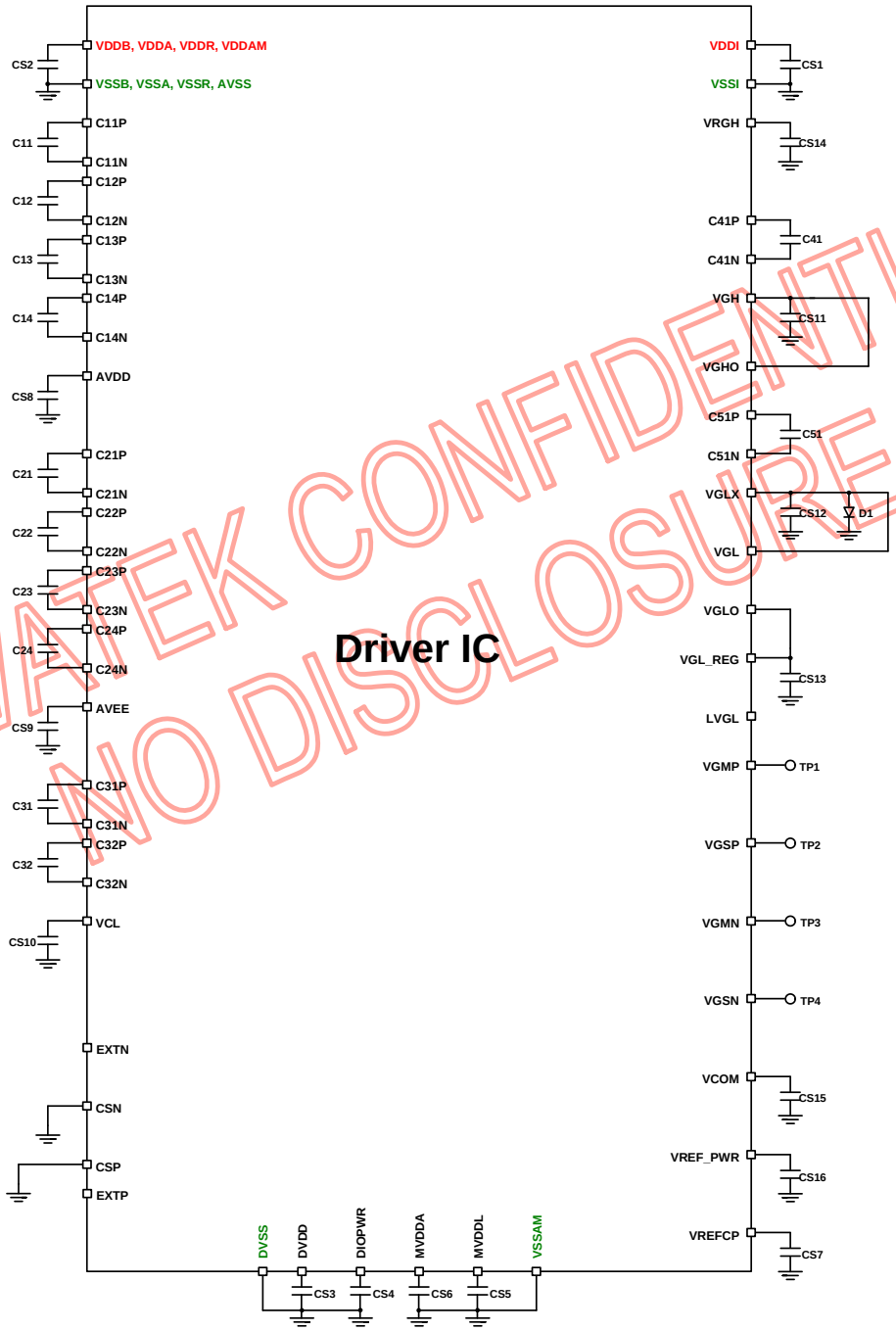
The boost voltage generated in NT35510 is shown as below.



2.2 DC/DC Converter Circuit

The DC-DC converter is highly efficient step-up voltage generator circuits that generate the high voltage level AVDD/AVEE required for source drivers and VGHO/VGLO required for gate control signals for panel.

- Using charge pump for AVDD/AVEE voltage and LVGL is used

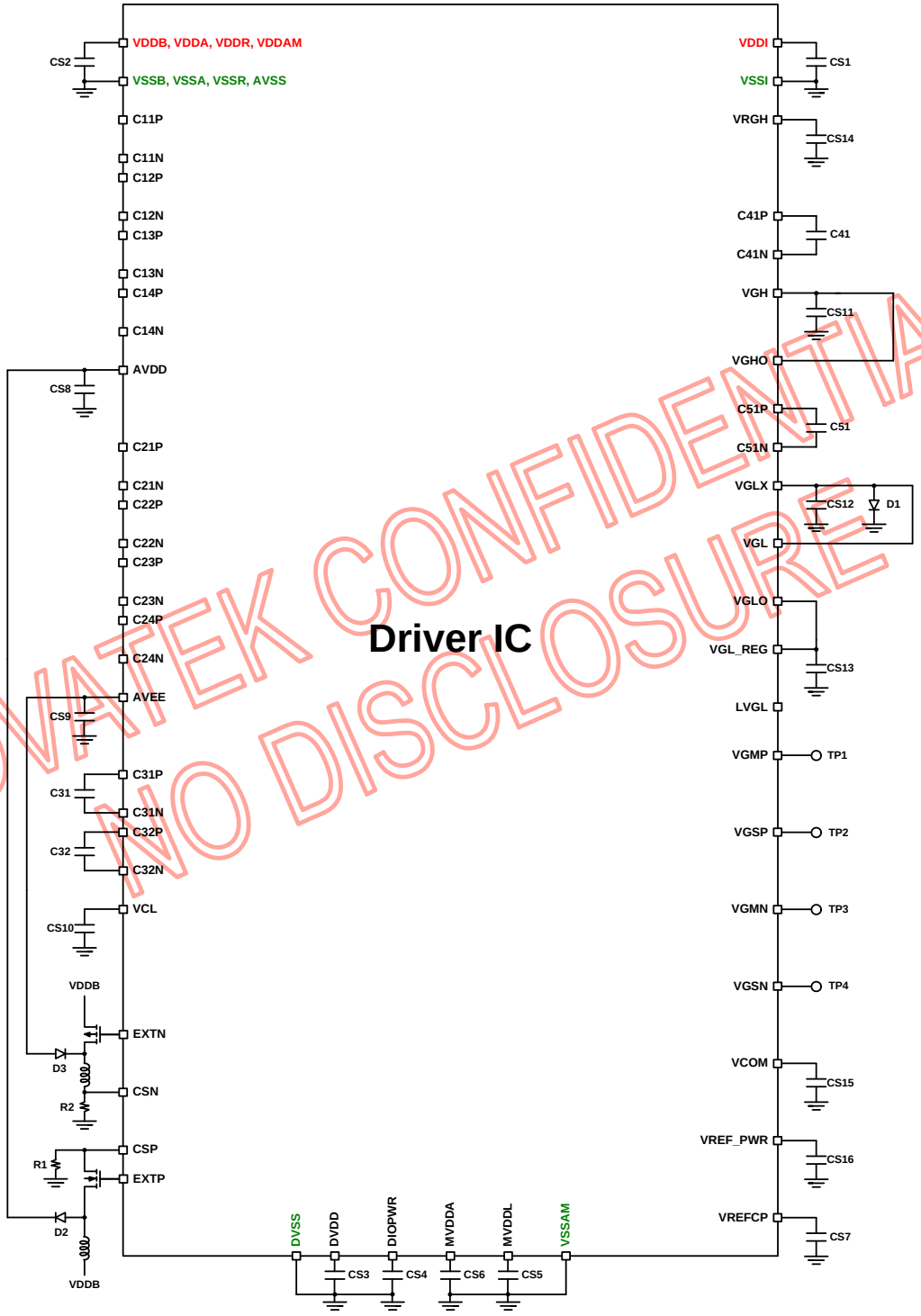


Notes:

1. VRGH (VBIAS voltage of panel) can be open if not used.

2. Input voltage VDDB=2.6~4.8V when using charge pump for AVDD/AVEE voltage.

- Using PFM for AVDD/AVEE voltage and LVGL is used



Note: VRGH (VBIAS voltage of panle) can be open if not used.

3 MAXIMUM SERIES RESISTANCE

The driver will operate in “Chip on Glass” applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in below table.

Name	Type	Maximum Series Resistance	Unit
VDDI	Power supply	10	Ω
VDDA, VDDR	Power supply	10	Ω
VDDB	Power supply	5	Ω
VDDAM	Power supply	10	Ω
DVDD	Power supply	10	Ω
DIOPWR, MVDDA, MVDDL	Power supply	10	Ω
VSSI	Power supply	10	Ω
DVSS	Power supply	10	Ω
VSSA, VSSR, AVSS	Power supply	10	Ω
VSSB	Power supply	5	Ω
VSSAM	Power supply	10	Ω
IM[3:0], VSEL, I2C_SA0, RGBBP, LANSEL, DSWAP, PSWAP, VGSW[3:0], NBWSEL, DSTB_SEL	Input	100	Ω
RESX	Input	50	Ω
CSX, WRX/SCL/I2C_SCL, RDX, SDI/I2C_SDA	Input	50	Ω
SDO, TE, ERR, GPO[3:0], LEDPWM, LEDON, KBBC	Output	50	Ω
D23 to D0	Input / Output	50	Ω
PCLK, DE, VS, HS	Input	50	Ω
HSSI_CLK_P/N, HSSI_DATA0_P/N, HSSI_DATA1_P/N	Input	10	Ω
VREF_PWR, VREFCP	Power output	10	Ω
VGMP, VGSP, VGMN, VGSN	Power output	10	Ω
VCOM	Capacitor connection	5	Ω
AVDD, AVEE, VCL	Capacitor connection	5	Ω
C11P/N~C14P/N	Capacitor connection	5	Ω
C21P/N~C24P/N	Capacitor connection	5	Ω
C31P/N~C32P/N	Capacitor connection	5	Ω
VGH, VGLX, VGL_REG	Capacitor connection	10	Ω
C41P/N, C51P/N	Capacitor connection	5	Ω
EXTP, EXTN	MOS connection	10	Ω
CSP, CSN	Resistor connection	20	Ω
MTP_PWR	Power supply	10	Ω

4 EXTERNAL COMPONENTS CONNECTION

- Using charge pump for AVDD/AVEE voltage and LVGL is used

Pad Name	Connection	Typical Value
VDDI	VDDI, connect to capacitor (Max 6V) VDDI ------||------ GND	1.0μF
VDDA, VDDR, VDDB, VDDAM	VDD2, connect to capacitor (Max 6V) VDD2 ------||------ GND	2.2~4.7μF
DVDD	Connect to Capacitor (Max 3V): DVDD ------||------ GND	1.0μF
DIOPWR	Connect to Capacitor (Max 3V): DIOPWR -----||----- GND	1.0μF
MVDDA	Connect to Capacitor (Max 3V): MVDDA ------||------ GND	1.0μF
MVDDL	Connect to Capacitor (Max 3V): MVDDL ------||------ GND	1.0μF
VSSI, DVSS	Interface and Digital ground (Connect to GND)	-
VSSB, VSSA, VSSR, AVSS	Analog ground (Connect to GND)	-
VSSAM	MIPI ground (Connect to GND)	-
C11P, C11N	Connect to Capacitor (Max 6V): C11P ------||------ C11N	1.0μF
C12P, C12N	Connect to Capacitor (Max 10V): C12P ------||------ C12N	1.0μF
C13P, C13N	Connect to Capacitor (Max 6V): C13P ------||------ C13N	1.0μF
C14P, C14N	Connect to Capacitor (Max 10V): C14P ------||------ C14N	1.0μF
C21P, C21N	Connect to Capacitor (Max 10V): C21P ------||------ C21N	1.0μF
C22P, C22N	Connect to Capacitor (Max 16V): C22P ------||------ C22N	1.0μF
C23P, C23N	Connect to Capacitor (Max 10V): C23P ------||------ C23N	1.0μF
C24P, C24N	Connect to Capacitor (Max 16V): C24P ------||------ C24N	1.0μF
C31P, C31N	Connect to Capacitor (Max 6V): C31P ------||------ C31N	1.0μF
C32P, C32N	Connect to Capacitor (Max 10V): C32P ------||------ C32N	1.0μF
C41P, C41N	Connect to Capacitor (Max 16V): C41P ------||------ C41N	1.0μF
C51P, C51N	Connect to Capacitor (Max 16V): C51P ------||------ C51N	1.0μF
AVDD	Connect to Capacitor (Max 10V): AVDD ------||------ GND	4.7μF
AVEE	Connect to Capacitor (Max 10V): AVEE ------||------ GND	4.7μF
VCL	Connect to Capacitor (Max 10V): VCL ------||------ GND	2.2μF
VGH	Connect to Capacitor (Max 25V): VGH ------||------ GND	2.2μF
VGLX, VGL	Connect to Capacitor (Max 25V): VGLX --------||-------- GND └-----►|------ GND └---------- VGL	2.2μF
VGL_REG	Connect to Capacitor (Max 25V): VGL_REG ------||------ GND	1.0μF
VRGH	Connect to Capacitor (Max 10V): VRGH ------||------ GND	1.0μF
VREFCP	Connect to Capacitor (Max 6V): VREFCP ------||------ GND	1.0μF
VCOM	Connect to Capacitor (Max 6V): VCOM ------||------ GND	2.2μF
VREF_PWR	Connect to Capacitor (Max 6V): VREF ------||------ GND	2.2μF
VGMP, VGSP, VGMN, VGSN	Test point on FPC for measurement purpose	-

NOTE: The specification of Schottky Diode: VF<0.4V at 100mA, VR>30V.
The recommended component: Panasonic MA27D29 (VF=0.39V@100mA and VR=30V).

- Using PFM for AVDD/AVEE voltage and LVGL is used

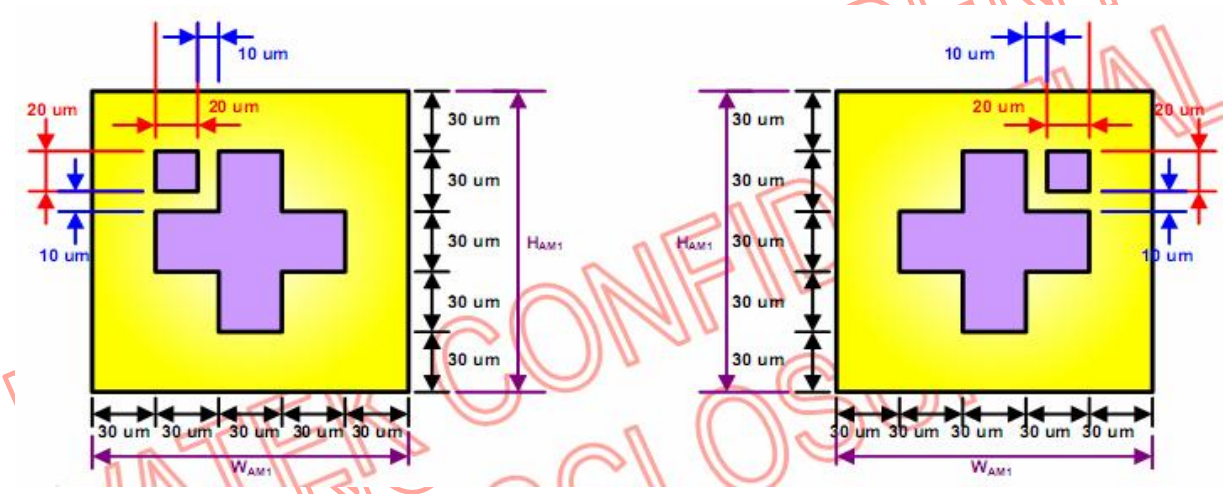
Pad Name	Connection	Typical Value
VDDI	VDDI, connect to capacitor (Max 6V) VDDI ------||------ GND	1.0μF
VDDA, VDDR, VDDB, VDDAM	VDD2, connect to capacitor (Max 6V) VDD2 ------||------ GND	2.2~4.7μF
DVDD	Connect to Capacitor (Max 6V): DVDD ------||------ GND	1.0μF
DIOPWR	Connect to Capacitor (Max 6V): DIOPWR -----||----- GND	1.0μF
MVDDA	Connect to Capacitor (Max 6V): MVDDA ------||------ GND	1.0μF
MVDDL	Connect to Capacitor (Max 6V): MVDDL ------||------ GND	1.0μF
VSSI, DVSS	Interface and Digital ground (Connect to GND)	-
VSSB, VSSA, VSSR, AVSS	Analog ground (Connect to GND)	-
VSSAM	MIPI ground (Connect to GND)	-
C31P, C31N	Connect to Capacitor (Max 6V): C31P ------||------ C31N	1.0μF
C32P, C32N	Connect to Capacitor (Max 10V): C32P ------||------ C32N	1.0μF
C41P, C41N	Connect to Capacitor (Max 16V): C41P ------||------ C41N	1.0μF
C51P, C51N	Connect to Capacitor (Max 16V): C51P ------||------ C51N	1.0μF
AVDD	Capacitor (Max 10V): AVDD -----||----- VSSB Shottky Diode1: AVDD -----|◄----- Drain-NMOS1 Inductor1: └---- L1 ----- VDDB	4.7μF
EXTP	NMOS1: EXTP ----- Gate-NMOS1	
CSP	NMOS1: CSP ----- Source-NMOS1 Resistor1: CSP ----- R1 ----- VSSB	0.1Ω
AVEE	Capacitor (Max 10V): AVEE -----||----- VSSB Schottky Diode2: AVEE -----►|----- Drain-PMOS1	4.7μF
EXTN	PMOS1: EXTN ----- Gate-PMOS2 Source-PMOS2 ----- VDDB	
CSN	Inductor2: CSN ----- L2 ----- Drain-PMOS2 Resistor2: └---- R2 ----- VSSB	0.1Ω
VCL	Connect to Capacitor (Max 6V): VCL ------||------ GND	2.2μF
VGH	Connect to Capacitor (Max 25V): VGH ------||------ GND	2.2μF
VGLX, VGL	Connect to Capacitor (Max 25V): VGLX --------||-------- GND └-----►|------ GND └---------- VGL	2.2μF
VGL_REG (can be open if not used)	Connect to Capacitor (Max 25V): VGL_REG ------||------ GND	1.0μF
VRGH (can be open if not used)	Connect to Capacitor (Max 10V): VRGH ------||------ GND	1.0μF
VREFCP	Connect to Capacitor (Max 6V): VREFCP ------||------ GND	1.0μF
VCOM	Connect to Capacitor (Max 6V): VCOM ------||------ GND	2.2μF
VREF_PWR	Connect to Capacitor (Max 6V): VREF_PWR ------||------ GND	2.2μF
VGMP, VGSP, VGMN, VGSN	Test point on FPC for measurement purpose	-

NOTE: The specification of Schottky Diode: VF<0.4V at 100mA, VR>30V.
The recommended component: Panasonic MA27D29 (VF=0.39V@100mA and VR=30V).

5 CHIP INFORMATION

5.1 Chip Overview

-Chip size (including scribe line): 24000μm x 1635μm.
-Chip thickness: 200 um
-PAD coordinate: PAD center
-Coordinate origin: Chip center
-Au bump size
  Input side: 40μm x 120μm
  Output side: 14μm x 115μm
-Alignment Mark coordinate
  ALMARK_R_T(11870, 687.5)
  ALMARK_L_T(-11870, 687.5)
-Alignment Mark size



ALK_L ALK_R

5.2 Pad Coordinates

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	VSSIDUM0	-11880	-702.5	51	TEST2	-8850	-702.5
2	VSSIDUM1	-11790	-702.5	52	TEST3	-8790	-702.5
3	PADA1	-11730	-702.5	53	VDD_DET	-8730	-702.5
4	PADB1	-11670	-702.5	54	DIOPWR	-8670	-702.5
5	VCOM	-11610	-702.5	55	DIOPWR	-8610	-702.5
6	VCOM	-11550	-702.5	56	VGSN	-8550	-702.5
7	VCOM	-11490	-702.5	57	VGSN_VGSP	-8490	-702.5
8	VCOM	-11430	-702.5	58	VGSP	-8430	-702.5
9	VCOM	-11370	-702.5	59	VGMN	-8370	-702.5
10	CONTACT1A	-11310	-702.5	60	VGMN_VGMP	-8310	-702.5
11	CONTACT1B	-11250	-702.5	61	VGMP	-8250	-702.5
12	MTP_PWR	-11190	-702.5	62	DVSS	-8190	-702.5
13	MTP_PWR	-11130	-702.5	63	DVSS	-8130	-702.5
14	MTP_PWR	-11070	-702.5	64	DVSS	-8070	-702.5
15	MTP_PWR	-11010	-702.5	65	DVDD	-8010	-702.5
16	MTP_PWR	-10950	-702.5	66	DVDD	-7950	-702.5
17	VGLX	-10890	-702.5	67	DVDD	-7890	-702.5
18	VGLX	-10830	-702.5	68	VDDB	-7830	-702.5
19	VGLO	-10770	-702.5	69	VDDB	-7770	-702.5
20	VGLO	-10710	-702.5	70	VDDB	-7710	-702.5
21	VGL_REG	-10650	-702.5	71	VCL_VDDB	-7650	-702.5
22	VGL_REG	-10590	-702.5	72	VCL_VDDB	-7590	-702.5
23	VRGH	-10530	-702.5	73	VCL	-7530	-702.5
24	VRGH	-10470	-702.5	74	VCL	-7470	-702.5
25	VCL	-10410	-702.5	75	VCL_AVSS	-7410	-702.5
26	VCL	-10350	-702.5	76	VCL_AVSS	-7350	-702.5
27	VCL	-10290	-702.5	77	AVSS	-7290	-702.5
28	VCL	-10230	-702.5	78	AVSS	-7230	-702.5
29	VREF_PWR	-10170	-702.5	79	AVSS	-7170	-702.5
30	VREF_PWR	-10110	-702.5	80	VDDI_OPT1	-7110	-702.5
31	VREF_PWR	-10050	-702.5	81	LANSEL	-7050	-702.5
32	VREF_PWR	-9990	-702.5	82	DSWAP	-6990	-702.5
33	VSSA	-9930	-702.5	83	PSWAP	-6930	-702.5
34	VSSA	-9870	-702.5	84	VSSI_OPT1	-6870	-702.5
35	VSSA	-9810	-702.5	85	DSTB_SEL	-6810	-702.5
36	VSSA	-9750	-702.5	86	NBWSEL	-6750	-702.5
37	VDDA	-9690	-702.5	87	VGSW3	-6690	-702.5
38	VDDA	-9630	-702.5	88	VGSW2	-6630	-702.5
39	VDDA	-9570	-702.5	89	VGSW1	-6570	-702.5
40	VDDA	-9510	-702.5	90	VGSW0	-6510	-702.5
41	VDDR	-9450	-702.5	91	VDDI_OPT2	-6450	-702.5
42	VDDR	-9390	-702.5	92	RGBBP	-6390	-702.5
43	VDDR	-9330	-702.5	93	I2C_SA0	-6330	-702.5
44	VDDR	-9270	-702.5	94	IM3	-6270	-702.5
45	VSSR	-9210	-702.5	95	IM2	-6210	-702.5
46	VSSR	-9150	-702.5	96	IM1	-6150	-702.5
47	VSSR	-9090	-702.5	97	IM0	-6090	-702.5
48	VSSR	-9030	-702.5	98	GPO3	-6030	-702.5
49	TEST0	-8970	-702.5	99	GPO2	-5970	-702.5
50	TEST1	-8910	-702.5	100	GPO1	-5910	-702.5

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
101	GPO0	-5850	-702.5	151	VDDI	-2850	-702.5
102	EXB1T	-5790	-702.5	152	VDDI	-2790	-702.5
103	TE_L	-5730	-702.5	153	VSSI	-2730	-702.5
104	VSEL	-5670	-702.5	154	VSSI	-2670	-702.5
105	SDO	-5610	-702.5	155	VSSI	-2610	-702.5
106	SDI	-5550	-702.5	156	AVDD	-2550	-702.5
107	DCX	-5490	-702.5	157	AVDD	-2490	-702.5
108	WRX	-5430	-702.5	158	AVDD	-2430	-702.5
109	RDX	-5370	-702.5	159	AVDD	-2370	-702.5
110	CSX	-5310	-702.5	160	AVSS_AVDD	-2310	-702.5
111	RESX	-5250	-702.5	161	AVSS_AVDD	-2250	-702.5
112	VSSI	-5190	-702.5	162	AVSS	-2190	-702.5
113	VSSI	-5130	-702.5	163	AVSS	-2130	-702.5
114	VSSI	-5070	-702.5	164	AVEE_AVSS	-2070	-702.5
115	VDDI	-5010	-702.5	165	AVEE_AVSS	-2010	-702.5
116	VDDI	-4950	-702.5	166	AVEE	-1950	-702.5
117	VDDI	-4890	-702.5	167	AVEE	-1890	-702.5
118	D23	-4830	-702.5	168	AVEE	-1830	-702.5
119	D22	-4770	-702.5	169	VDDA	-1770	-702.5
120	D21	-4710	-702.5	170	VDDA	-1710	-702.5
121	D20	-4650	-702.5	171	VDDA	-1650	-702.5
122	D19	-4590	-702.5	172	VDDA	-1590	-702.5
123	D18	-4530	-702.5	173	DVSS	-1530	-702.5
124	D17	-4470	-702.5	174	DVSS	-1470	-702.5
125	D16	-4410	-702.5	175	DVSS	-1410	-702.5
126	D15	-4350	-702.5	176	DVSS	-1350	-702.5
127	D14	-4290	-702.5	177	DVDD	-1290	-702.5
128	D13	-4230	-702.5	178	DVDD	-1230	-702.5
129	D12	-4170	-702.5	179	DVDD	-1170	-702.5
130	D11	-4110	-702.5	180	DVDD	-1110	-702.5
131	D10	-4050	-702.5	181	VSSAM	-1050	-702.5
132	D9	-3990	-702.5	182	VSSAM	-990	-702.5
133	D8	-3930	-702.5	183	VSSAM	-930	-702.5
134	D7	-3870	-702.5	184	VSSAM	-870	-702.5
135	D6	-3810	-702.5	185	VSSAM	-810	-702.5
136	D5	-3750	-702.5	186	HSSI_D1_P	-750	-702.5
137	D4	-3690	-702.5	187	HSSI_D1_P	-690	-702.5
138	D3	-3630	-702.5	188	HSSI_D1_P	-630	-702.5
139	D2	-3570	-702.5	189	HSSI_D1_P	-570	-702.5
140	D1	-3510	-702.5	190	HSSI_D1_N	-510	-702.5
141	D0	-3450	-702.5	191	HSSI_D1_N	-450	-702.5
142	DE	-3390	-702.5	192	HSSI_D1_N	-390	-702.5
143	PCLK	-3330	-702.5	193	HSSI_D1_N	-330	-702.5
144	HS	-3270	-702.5	194	VSSAM	-270	-702.5
145	VS	-3210	-702.5	195	VSSAM	-210	-702.5
146	LEDPWM	-3150	-702.5	196	HSSI_CLK_P	-150	-702.5
147	LEDON	-3090	-702.5	197	HSSI_CLK_P	-90	-702.5
148	KBBC	-3030	-702.5	198	HSSI_CLK_P	-30	-702.5
149	ERR	-2970	-702.5	199	HSSI_CLK_P	30	-702.5
150	VDDI	-2910	-702.5	200	HSSI_CLK_N	90	-702.5

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
201	HSSI_CLK_N	150	-702.5	251	VDDB	3150	-702.5
202	HSSI_CLK_N	210	-702.5	252	VDDB	3210	-702.5
203	HSSI_CLK_N	270	-702.5	253	VDDB	3270	-702.5
204	VSSAM	330	-702.5	254	VSSB	3330	-702.5
205	VSSAM	390	-702.5	255	VSSB	3390	-702.5
206	HSSI_D0_P	450	-702.5	256	VSSB	3450	-702.5
207	HSSI_D0_P	510	-702.5	257	VSSB	3510	-702.5
208	HSSI_D0_P	570	-702.5	258	VSSB	3570	-702.5
209	HSSI_D0_P	630	-702.5	259	VSSB	3630	-702.5
210	HSSI_D0_N	690	-702.5	260	C11P	3690	-702.5
211	HSSI_D0_N	750	-702.5	261	C11P	3750	-702.5
212	HSSI_D0_N	810	-702.5	262	C11P	3810	-702.5
213	HSSI_D0_N	870	-702.5	263	C11N	3870	-702.5
214	VSSAM	930	-702.5	264	C11N	3930	-702.5
215	VSSAM	990	-702.5	265	C11N	3990	-702.5
216	MVDDL	1050	-702.5	266	C12P	4050	-702.5
217	MVDDL	1110	-702.5	267	C12P	4110	-702.5
218	MVDDL	1170	-702.5	268	C12P	4170	-702.5
219	MVDDA	1230	-702.5	269	C12N	4230	-702.5
220	MVDDA	1290	-702.5	270	C12N	4290	-702.5
221	MVDDA	1350	-702.5	271	C12N	4350	-702.5
222	VDDAM	1410	-702.5	272	C13P	4410	-702.5
223	VDDAM	1470	-702.5	273	C13P	4470	-702.5
224	VDDAM	1530	-702.5	274	C13P	4530	-702.5
225	VDDAM	1590	-702.5	275	C13N	4590	-702.5
226	VDDAM	1650	-702.5	276	C13N	4650	-702.5
227	VDDR	1710	-702.5	277	C13N	4710	-702.5
228	VDDR	1770	-702.5	278	C14P	4770	-702.5
229	VDDR	1830	-702.5	279	C14P	4830	-702.5
230	OSC_TEST	1890	-702.5	280	C14P	4890	-702.5
231	TE_R	1950	-702.5	281	C14N	4950	-702.5
232	VSSR	2010	-702.5	282	C14N	5010	-702.5
233	VSSR	2070	-702.5	283	C14N	5070	-702.5
234	VSSR	2130	-702.5	284	AVDD	5130	-702.5
235	VSSR	2190	-702.5	285	AVDD	5190	-702.5
236	VREFCP	2250	-702.5	286	AVDD	5250	-702.5
237	VREFCP	2310	-702.5	287	AVDD	5310	-702.5
238	VRGH	2370	-702.5	288	AVSS_AVDD	5370	-702.5
239	VRGH	2430	-702.5	289	AVSS_AVDD	5430	-702.5
240	EXTP	2490	-702.5	290	AVSS	5490	-702.5
241	EXTP	2550	-702.5	291	AVSS	5550	-702.5
242	CSP	2610	-702.5	292	AVSS	5610	-702.5
243	CSP	2670	-702.5	293	AVEE_AVSS	5670	-702.5
244	EXTN	2730	-702.5	294	AVEE_AVSS	5730	-702.5
245	EXTN	2790	-702.5	295	AVEE	5790	-702.5
246	CSN	2850	-702.5	296	AVEE	5850	-702.5
247	CSN	2910	-702.5	297	AVEE	5910	-702.5
248	VDDB	2970	-702.5	298	AVEE	5970	-702.5
249	VDDB	3030	-702.5	299	C21P	6030	-702.5
250	VDDB	3090	-702.5	300	C21P	6090	-702.5

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
301	C21P	6150	-702.5	351	C32N	9150	-702.5
302	C21N	6210	-702.5	352	C32N	9210	-702.5
303	C21N	6270	-702.5	353	C32N	9270	-702.5
304	C21N	6330	-702.5	354	DVDD	9330	-702.5
305	C22P	6390	-702.5	355	DVDD	9390	-702.5
306	C22P	6450	-702.5	356	DVDD	9450	-702.5
307	C22P	6510	-702.5	357	DVSS	9510	-702.5
308	C22N	6570	-702.5	358	DVSS	9570	-702.5
309	C22N	6630	-702.5	359	DVSS	9630	-702.5
310	C22N	6690	-702.5	360	C41P	9690	-702.5
311	C23P	6750	-702.5	361	C41P	9750	-702.5
312	C23P	6810	-702.5	362	C41N	9810	-702.5
313	C23P	6870	-702.5	363	C41N	9870	-702.5
314	C23N	6930	-702.5	364	VGH	9930	-702.5
315	C23N	6990	-702.5	365	VGH	9990	-702.5
316	C23N	7050	-702.5	366	VGHO	10050	-702.5
317	C24P	7110	-702.5	367	VGHO	10110	-702.5
318	C24P	7170	-702.5	368	VRGH	10170	-702.5
319	C24P	7230	-702.5	369	VRGH	10230	-702.5
320	C24N	7290	-702.5	370	C51P	10290	-702.5
321	C24N	7350	-702.5	371	C51P	10350	-702.5
322	C24N	7410	-702.5	372	C51N	10410	-702.5
323	VDDB	7470	-702.5	373	C51N	10470	-702.5
324	VDDB	7530	-702.5	374	VGL_REG	10530	-702.5
325	VDDB	7590	-702.5	375	VGL_REG	10590	-702.5
326	VDDB	7650	-702.5	376	VGLO	10650	-702.5
327	VDDB	7710	-702.5	377	VGLO	10710	-702.5
328	VCL_VDDB	7770	-702.5	378	VGLX	10770	-702.5
329	VCL_VDDB	7830	-702.5	379	VGLX	10830	-702.5
330	VCL	7890	-702.5	380	VGL	10890	-702.5
331	VCL	7950	-702.5	381	VGL	10950	-702.5
332	VCL	8010	-702.5	382	TEST4	11010	-702.5
333	VCL_AVSS	8070	-702.5	383	TEST5	11070	-702.5
334	VCL_AVSS	8130	-702.5	384	TEST6	11130	-702.5
335	AVSS	8190	-702.5	385	TEST7	11190	-702.5
336	AVSS	8250	-702.5	386	CONTACT2A	11250	-702.5
337	AVSS	8310	-702.5	387	CONTACT2B	11310	-702.5
338	VSSB	8370	-702.5	388	VCOM	11370	-702.5
339	VSSB	8430	-702.5	389	VCOM	11430	-702.5
340	VSSB	8490	-702.5	390	VCOM	11490	-702.5
341	VSSB	8550	-702.5	391	VCOM	11550	-702.5
342	C31P	8610	-702.5	392	VCOM	11610	-702.5
343	C31P	8670	-702.5	393	PADA2	11670	-702.5
344	C31P	8730	-702.5	394	PADB2	11730	-702.5
345	C31N	8790	-702.5	395	VSSIDUM2	11790	-702.5
346	C31N	8850	-702.5	396	VSSIDUM3	11880	-702.5
347	C31N	8910	-702.5	397	VSSIDUM4	11760	705
348	C32P	8970	-702.5	398	VSSIDUM5	11732	560
349	C32P	9030	-702.5	399	VSSIDUM6	11718	705
350	C32P	9090	-702.5	400	PADA3	11704	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
401	PADB3	11690	705	451	VGHO	10990	705
402	VGHO	11676	560	452	VGHO	10976	560
403	VGHO	11662	705	453	VGHO	10962	705
404	VGHO	11648	560	454	VGHO	10948	560
405	VGLO	11634	705	455	VGHO	10934	705
406	VGLO	11620	560	456	VGHO	10920	560
407	VGLO	11606	705	457	VGLO	10906	705
408	GOUT1	11592	560	458	VGLO	10892	560
409	GOUT1	11578	705	459	VGLO	10878	705
410	GOUT2	11564	560	460	VGLO	10864	560
411	GOUT2	11550	705	461	VGLO	10850	705
412	LVGL	11536	560	462	VGLO	10836	560
413	LVGL	11522	705	463	VGLO	10822	705
414	LVGL	11508	560	464	VGLO	10808	560
415	VRGH	11494	705	465	VGLO	10794	705
416	VRGH	11480	560	466	VSSIDUM7	10780	560
417	VRGH	11466	705	467	VSSIDUM8	10766	705
418	VGLO	11452	560	468	SDUM0	10752	560
419	VGLO	11438	705	469	SDUM1	10738	705
420	VGLO	11424	560	470	S1	10724	560
421	GOUT3	11410	705	471	S2	10710	705
422	GOUT3	11396	560	472	S3	10696	560
423	GOUT4	11382	705	473	S4	10682	705
424	GOUT4	11368	560	474	S5	10668	560
425	GOUT5	11354	705	475	S6	10654	705
426	GOUT5	11340	560	476	S7	10640	560
427	GOUT6	11326	705	477	S8	10626	705
428	GOUT6	11312	560	478	S9	10612	560
429	GOUT7	11298	705	479	S10	10598	705
430	GOUT7	11284	560	480	S11	10584	560
431	GOUT8	11270	705	481	S12	10570	705
432	GOUT8	11256	560	482	S13	10556	560
433	GOUT9	11242	705	483	S14	10542	705
434	GOUT9	11228	560	484	S15	10528	560
435	GOUT10	11214	705	485	S16	10514	705
436	GOUT10	11200	560	486	S17	10500	560
437	GOUT11	11186	705	487	S18	10486	705
438	GOUT11	11172	560	488	S19	10472	560
439	GOUT12	11158	705	489	S20	10458	705
440	GOUT12	11144	560	490	S21	10444	560
441	GOUT13	11130	705	491	S22	10430	705
442	GOUT13	11116	560	492	S23	10416	560
443	GOUT14	11102	705	493	S24	10402	705
444	GOUT14	11088	560	494	S25	10388	560
445	GOUT15	11074	705	495	S26	10374	705
446	GOUT15	11060	560	496	S27	10360	560
447	GOUT16	11046	705	497	S28	10346	705
448	GOUT16	11032	560	498	S29	10332	560
449	VGHO	11018	705	499	S30	10318	705
450	VGHO	11004	560	500	S31	10304	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
501	S32	10290	705	551	S82	9590	705
502	S33	10276	560	552	S83	9576	560
503	S34	10262	705	553	S84	9562	705
504	S35	10248	560	554	S85	9548	560
505	S36	10234	705	555	S86	9534	705
506	S37	10220	560	556	S87	9520	560
507	S38	10206	705	557	S88	9506	705
508	S39	10192	560	558	S89	9492	560
509	S40	10178	705	559	S90	9478	705
510	S41	10164	560	560	S91	9464	560
511	S42	10150	705	561	S92	9450	705
512	S43	10136	560	562	S93	9436	560
513	S44	10122	705	563	S94	9422	705
514	S45	10108	560	564	S95	9408	560
515	S46	10094	705	565	S96	9394	705
516	S47	10080	560	566	S97	9380	560
517	S48	10066	705	567	S98	9366	705
518	S49	10052	560	568	S99	9352	560
519	S50	10038	705	569	S100	9338	705
520	S51	10024	560	570	S101	9324	560
521	S52	10010	705	571	S102	9310	705
522	S53	9996	560	572	S103	9296	560
523	S54	9982	705	573	S104	9282	705
524	S55	9968	560	574	S105	9268	560
525	S56	9954	705	575	S106	9254	705
526	S57	9940	560	576	S107	9240	560
527	S58	9926	705	577	S108	9226	705
528	S59	9912	560	578	S109	9212	560
529	S60	9898	705	579	S110	9198	705
530	S61	9884	560	580	S111	9184	560
531	S62	9870	705	581	S112	9170	705
532	S63	9856	560	582	S113	9156	560
533	S64	9842	705	583	S114	9142	705
534	S65	9828	560	584	S115	9128	560
535	S66	9814	705	585	S116	9114	705
536	S67	9800	560	586	S117	9100	560
537	S68	9786	705	587	S118	9086	705
538	S69	9772	560	588	S119	9072	560
539	S70	9758	705	589	S120	9058	705
540	S71	9744	560	590	S121	9044	560
541	S72	9730	705	591	S122	9030	705
542	S73	9716	560	592	S123	9016	560
543	S74	9702	705	593	S124	9002	705
544	S75	9688	560	594	S125	8988	560
545	S76	9674	705	595	S126	8974	705
546	S77	9660	560	596	S127	8960	560
547	S78	9646	705	597	S128	8946	705
548	S79	9632	560	598	S129	8932	560
549	S80	9618	705	599	S130	8918	705
550	S81	9604	560	600	S131	8904	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
601	S132	8890	705	651	S182	8190	705
602	S133	8876	560	652	S183	8176	560
603	S134	8862	705	653	S184	8162	705
604	S135	8848	560	654	S185	8148	560
605	S136	8834	705	655	S186	8134	705
606	S137	8820	560	656	S187	8120	560
607	S138	8806	705	657	S188	8106	705
608	S139	8792	560	658	S189	8092	560
609	S140	8778	705	659	S190	8078	705
610	S141	8764	560	660	S191	8064	560
611	S142	8750	705	661	S192	8050	705
612	S143	8736	560	662	S193	8036	560
613	S144	8722	705	663	S194	8022	705
614	S145	8708	560	664	S195	8008	560
615	S146	8694	705	665	S196	7994	705
616	S147	8680	560	666	S197	7980	560
617	S148	8666	705	667	S198	7966	705
618	S149	8652	560	668	S199	7952	560
619	S150	8638	705	669	S200	7938	705
620	S151	8624	560	670	S201	7924	560
621	S152	8610	705	671	S202	7910	705
622	S153	8596	560	672	S203	7896	560
623	S154	8582	705	673	S204	7882	705
624	S155	8568	560	674	S205	7868	560
625	S156	8554	705	675	S206	7854	705
626	S157	8540	560	676	S207	7840	560
627	S158	8526	705	677	S208	7826	705
628	S159	8512	560	678	S209	7812	560
629	S160	8498	705	679	S210	7798	705
630	S161	8484	560	680	S211	7784	560
631	S162	8470	705	681	S212	7770	705
632	S163	8456	560	682	S213	7756	560
633	S164	8442	705	683	S214	7742	705
634	S165	8428	560	684	S215	7728	560
635	S166	8414	705	685	S216	7714	705
636	S167	8400	560	686	S217	7700	560
637	S168	8386	705	687	S218	7686	705
638	S169	8372	560	688	S219	7672	560
639	S170	8358	705	689	S220	7658	705
640	S171	8344	560	690	S221	7644	560
641	S172	8330	705	691	S222	7630	705
642	S173	8316	560	692	S223	7616	560
643	S174	8302	705	693	S224	7602	705
644	S175	8288	560	694	S225	7588	560
645	S176	8274	705	695	S226	7574	705
646	S177	8260	560	696	S227	7560	560
647	S178	8246	705	697	S228	7546	705
648	S179	8232	560	698	S229	7532	560
649	S180	8218	705	699	S230	7518	705
650	S181	8204	560	700	S231	7504	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
701	S232	7490	705	751	S282	6790	705
702	S233	7476	560	752	S283	6776	560
703	S234	7462	705	753	S284	6762	705
704	S235	7448	560	754	S285	6748	560
705	S236	7434	705	755	S286	6734	705
706	S237	7420	560	756	S287	6720	560
707	S238	7406	705	757	S288	6706	705
708	S239	7392	560	758	S289	6692	560
709	S240	7378	705	759	S290	6678	705
710	S241	7364	560	760	S291	6664	560
711	S242	7350	705	761	S292	6650	705
712	S243	7336	560	762	S293	6636	560
713	S244	7322	705	763	S294	6622	705
714	S245	7308	560	764	S295	6608	560
715	S246	7294	705	765	S296	6594	705
716	S247	7280	560	766	S297	6580	560
717	S248	7266	705	767	S298	6566	705
718	S249	7252	560	768	S299	6552	560
719	S250	7238	705	769	S300	6538	705
720	S251	7224	560	770	S301	6524	560
721	S252	7210	705	771	S302	6510	705
722	S253	7196	560	772	S303	6496	560
723	S254	7182	705	773	S304	6482	705
724	S255	7168	560	774	S305	6468	560
725	S256	7154	705	775	S306	6454	705
726	S257	7140	560	776	S307	6440	560
727	S258	7126	705	777	S308	6426	705
728	S259	7112	560	778	S309	6412	560
729	S260	7098	705	779	S310	6398	705
730	S261	7084	560	780	S311	6384	560
731	S262	7070	705	781	S312	6370	705
732	S263	7056	560	782	S313	6356	560
733	S264	7042	705	783	S314	6342	705
734	S265	7028	560	784	S315	6328	560
735	S266	7014	705	785	S316	6314	705
736	S267	7000	560	786	S317	6300	560
737	S268	6986	705	787	S318	6286	705
738	S269	6972	560	788	S319	6272	560
739	S270	6958	705	789	S320	6258	705
740	S271	6944	560	790	S321	6244	560
741	S272	6930	705	791	S322	6230	705
742	S273	6916	560	792	S323	6216	560
743	S274	6902	705	793	S324	6202	705
744	S275	6888	560	794	S325	6188	560
745	S276	6874	705	795	S326	6174	705
746	S277	6860	560	796	S327	6160	560
747	S278	6846	705	797	S328	6146	705
748	S279	6832	560	798	S329	6132	560
749	S280	6818	705	799	S330	6118	705
750	S281	6804	560	800	S331	6104	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
801	S332	6090	705	851	S382	5390	705
802	S333	6076	560	852	S383	5376	560
803	S334	6062	705	853	S384	5362	705
804	S335	6048	560	854	S385	5348	560
805	S336	6034	705	855	S386	5334	705
806	S337	6020	560	856	S387	5320	560
807	S338	6006	705	857	S388	5306	705
808	S339	5992	560	858	S389	5292	560
809	S340	5978	705	859	S390	5278	705
810	S341	5964	560	860	S391	5264	560
811	S342	5950	705	861	S392	5250	705
812	S343	5936	560	862	S393	5236	560
813	S344	5922	705	863	S394	5222	705
814	S345	5908	560	864	S395	5208	560
815	S346	5894	705	865	S396	5194	705
816	S347	5880	560	866	S397	5180	560
817	S348	5866	705	867	S398	5166	705
818	S349	5852	560	868	S399	5152	560
819	S350	5838	705	869	S400	5138	705
820	S351	5824	560	870	S401	5124	560
821	S352	5810	705	871	S402	5110	705
822	S353	5796	560	872	S403	5096	560
823	S354	5782	705	873	S404	5082	705
824	S355	5768	560	874	S405	5068	560
825	S356	5754	705	875	S406	5054	705
826	S357	5740	560	876	S407	5040	560
827	S358	5726	705	877	S408	5026	705
828	S359	5712	560	878	S409	5012	560
829	S360	5698	705	879	S410	4998	705
830	S361	5684	560	880	S411	4984	560
831	S362	5670	705	881	S412	4970	705
832	S363	5656	560	882	S413	4956	560
833	S364	5642	705	883	S414	4942	705
834	S365	5628	560	884	S415	4928	560
835	S366	5614	705	885	S416	4914	705
836	S367	5600	560	886	S417	4900	560
837	S368	5586	705	887	S418	4886	705
838	S369	5572	560	888	S419	4872	560
839	S370	5558	705	889	S420	4858	705
840	S371	5544	560	890	S421	4844	560
841	S372	5530	705	891	S422	4830	705
842	S373	5516	560	892	S423	4816	560
843	S374	5502	705	893	S424	4802	705
844	S375	5488	560	894	S425	4788	560
845	S376	5474	705	895	S426	4774	705
846	S377	5460	560	896	S427	4760	560
847	S378	5446	705	897	S428	4746	705
848	S379	5432	560	898	S429	4732	560
849	S380	5418	705	899	S430	4718	705
850	S381	5404	560	900	S431	4704	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
901	S432	4690	705	951	S482	3990	705
902	S433	4676	560	952	S483	3976	560
903	S434	4662	705	953	S484	3962	705
904	S435	4648	560	954	S485	3948	560
905	S436	4634	705	955	S486	3934	705
906	S437	4620	560	956	S487	3920	560
907	S438	4606	705	957	S488	3906	705
908	S439	4592	560	958	S489	3892	560
909	S440	4578	705	959	S490	3878	705
910	S441	4564	560	960	S491	3864	560
911	S442	4550	705	961	S492	3850	705
912	S443	4536	560	962	S493	3836	560
913	S444	4522	705	963	S494	3822	705
914	S445	4508	560	964	S495	3808	560
915	S446	4494	705	965	S496	3794	705
916	S447	4480	560	966	S497	3780	560
917	S448	4466	705	967	S498	3766	705
918	S449	4452	560	968	S499	3752	560
919	S450	4438	705	969	S500	3738	705
920	S451	4424	560	970	S501	3724	560
921	S452	4410	705	971	S502	3710	705
922	S453	4396	560	972	S503	3696	560
923	S454	4382	705	973	S504	3682	705
924	S455	4368	560	974	S505	3668	560
925	S456	4354	705	975	S506	3654	705
926	S457	4340	560	976	S507	3640	560
927	S458	4326	705	977	S508	3626	705
928	S459	4312	560	978	S509	3612	560
929	S460	4298	705	979	S510	3598	705
930	S461	4284	560	980	S511	3584	560
931	S462	4270	705	981	S512	3570	705
932	S463	4256	560	982	S513	3556	560
933	S464	4242	705	983	S514	3542	705
934	S465	4228	560	984	S515	3528	560
935	S466	4214	705	985	S516	3514	705
936	S467	4200	560	986	S517	3500	560
937	S468	4186	705	987	S518	3486	705
938	S469	4172	560	988	S519	3472	560
939	S470	4158	705	989	S520	3458	705
940	S471	4144	560	990	S521	3444	560
941	S472	4130	705	991	S522	3430	705
942	S473	4116	560	992	S523	3416	560
943	S474	4102	705	993	S524	3402	705
944	S475	4088	560	994	S525	3388	560
945	S476	4074	705	995	S526	3374	705
946	S477	4060	560	996	S527	3360	560
947	S478	4046	705	997	S528	3346	705
948	S479	4032	560	998	S529	3332	560
949	S480	4018	705	999	S530	3318	705
950	S481	4004	560	1000	S531	3304	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1001	S532	3290	705	1051	S582	2590	705
1002	S533	3276	560	1052	S583	2576	560
1003	S534	3262	705	1053	S584	2562	705
1004	S535	3248	560	1054	S585	2548	560
1005	S536	3234	705	1055	S586	2534	705
1006	S537	3220	560	1056	S587	2520	560
1007	S538	3206	705	1057	S588	2506	705
1008	S539	3192	560	1058	S589	2492	560
1009	S540	3178	705	1059	S590	2478	705
1010	S541	3164	560	1060	S591	2464	560
1011	S542	3150	705	1061	S592	2450	705
1012	S543	3136	560	1062	S593	2436	560
1013	S544	3122	705	1063	S594	2422	705
1014	S545	3108	560	1064	S595	2408	560
1015	S546	3094	705	1065	S596	2394	705
1016	S547	3080	560	1066	S597	2380	560
1017	S548	3066	705	1067	S598	2366	705
1018	S549	3052	560	1068	S599	2352	560
1019	S550	3038	705	1069	S600	2338	705
1020	S551	3024	560	1070	S601	2324	560
1021	S552	3010	705	1071	S602	2310	705
1022	S553	2996	560	1072	S603	2296	560
1023	S554	2982	705	1073	S604	2282	705
1024	S555	2968	560	1074	S605	2268	560
1025	S556	2954	705	1075	S606	2254	705
1026	S557	2940	560	1076	S607	2240	560
1027	S558	2926	705	1077	S608	2226	705
1028	S559	2912	560	1078	S609	2212	560
1029	S560	2898	705	1079	S610	2198	705
1030	S561	2884	560	1080	S611	2184	560
1031	S562	2870	705	1081	S612	2170	705
1032	S563	2856	560	1082	S613	2156	560
1033	S564	2842	705	1083	S614	2142	705
1034	S565	2828	560	1084	S615	2128	560
1035	S566	2814	705	1085	S616	2114	705
1036	S567	2800	560	1086	S617	2100	560
1037	S568	2786	705	1087	S618	2086	705
1038	S569	2772	560	1088	S619	2072	560
1039	S570	2758	705	1089	S620	2058	705
1040	S571	2744	560	1090	S621	2044	560
1041	S572	2730	705	1091	S622	2030	705
1042	S573	2716	560	1092	S623	2016	560
1043	S574	2702	705	1093	S624	2002	705
1044	S575	2688	560	1094	S625	1988	560
1045	S576	2674	705	1095	S626	1974	705
1046	S577	2660	560	1096	S627	1960	560
1047	S578	2646	705	1097	S628	1946	705
1048	S579	2632	560	1098	S629	1932	560
1049	S580	2618	705	1099	S630	1918	705
1050	S581	2604	560	1100	S631	1904	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1101	S632	1890	705	1151	S682	1190	705
1102	S633	1876	560	1152	S683	1176	560
1103	S634	1862	705	1153	S684	1162	705
1104	S635	1848	560	1154	S685	1148	560
1105	S636	1834	705	1155	S686	1134	705
1106	S637	1820	560	1156	S687	1120	560
1107	S638	1806	705	1157	S688	1106	705
1108	S639	1792	560	1158	S689	1092	560
1109	S640	1778	705	1159	S690	1078	705
1110	S641	1764	560	1160	S691	1064	560
1111	S642	1750	705	1161	S692	1050	705
1112	S643	1736	560	1162	S693	1036	560
1113	S644	1722	705	1163	S694	1022	705
1114	S645	1708	560	1164	S695	1008	560
1115	S646	1694	705	1165	S696	994	705
1116	S647	1680	560	1166	S697	980	560
1117	S648	1666	705	1167	S698	966	705
1118	S649	1652	560	1168	S699	952	560
1119	S650	1638	705	1169	S700	938	705
1120	S651	1624	560	1170	S701	924	560
1121	S652	1610	705	1171	S702	910	705
1122	S653	1596	560	1172	S703	896	560
1123	S654	1582	705	1173	S704	882	705
1124	S655	1568	560	1174	S705	868	560
1125	S656	1554	705	1175	S706	854	705
1126	S657	1540	560	1176	S707	840	560
1127	S658	1526	705	1177	S708	826	705
1128	S659	1512	560	1178	S709	812	560
1129	S660	1498	705	1179	S710	798	705
1130	S661	1484	560	1180	S711	784	560
1131	S662	1470	705	1181	S712	770	705
1132	S663	1456	560	1182	S713	756	560
1133	S664	1442	705	1183	S714	742	705
1134	S665	1428	560	1184	S715	728	560
1135	S666	1414	705	1185	S716	714	705
1136	S667	1400	560	1186	S717	700	560
1137	S668	1386	705	1187	S718	686	705
1138	S669	1372	560	1188	S719	672	560
1139	S670	1358	705	1189	S720	658	705
1140	S671	1344	560	1190	VSSIDUM9	644	560
1141	S672	1330	705	1191	VSSIDUM10	630	705
1142	S673	1316	560	1192	VSSIDUM11	616	560
1143	S674	1302	705	1193	VSSIDUM12	602	705
1144	S675	1288	560	1194	VSSIDUM13	588	560
1145	S676	1274	705	1195	VSSIDUM14	574	705
1146	S677	1260	560	1196	VSSIDUM15	560	560
1147	S678	1246	705	1197	VSSIDUM16	546	705
1148	S679	1232	560	1198	VSSIDUM17	532	560
1149	S680	1218	705	1199	VSSIDUM18	518	705
1150	S681	1204	560	1200	VSSIDUM19	504	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1201	VSSIDUM20	490	705	1251	S733	-210	705
1202	VSSIDUM21	476	560	1252	S734	-224	560
1203	VSSIDUM22	462	705	1253	S735	-238	705
1204	VSSIDUM23	448	560	1254	S736	-252	560
1205	VSSIDUM24	434	705	1255	S737	-266	705
1206	VSSIDUM25	420	560	1256	S738	-280	560
1207	VSSIDUM26	406	705	1257	S739	-294	705
1208	VSSIDUM27	392	560	1258	S740	-308	560
1209	VSSIDUM28	378	705	1259	S741	-322	705
1210	VSSIDUM29	364	560	1260	S742	-336	560
1211	VSSIDUM30	350	705	1261	S743	-350	705
1212	VSSIDUM31	336	560	1262	S744	-364	560
1213	VSSIDUM32	322	705	1263	S745	-378	705
1214	VSSIDUM33	308	560	1264	S746	-392	560
1215	VSSIDUM34	294	705	1265	S747	-406	705
1216	VSSIDUM35	280	560	1266	S748	-420	560
1217	VSSIDUM36	266	705	1267	S749	-434	705
1218	VSSIDUM37	252	560	1268	S750	-448	560
1219	VSSIDUM38	238	705	1269	S751	-462	705
1220	VSSIDUM39	224	560	1270	S752	-476	560
1221	VSSIDUM40	210	705	1271	S753	-490	705
1222	VSSIDUM41	196	560	1272	S754	-504	560
1223	VSSIDUM42	182	705	1273	S755	-518	705
1224	VSSIDUM43	168	560	1274	S756	-532	560
1225	VSSIDUM44	154	705	1275	S757	-546	705
1226	VSSIDUM45	140	560	1276	S758	-560	560
1227	VSSIDUM46	126	705	1277	S759	-574	705
1228	VSSIDUM47	112	560	1278	S760	-588	560
1229	VSSIDUM48	98	705	1279	S761	-602	705
1230	VSSIDUM49	84	560	1280	S762	-616	560
1231	VSSIDUM50	70	705	1281	S763	-630	705
1232	VSSIDUM51	56	560	1282	S764	-644	560
1233	VSSIDUM52	42	705	1283	S765	-658	705
1234	VSSIDUM53	28	560	1284	S766	-672	560
1235	VSSIDUM54	14	705	1285	S767	-686	705
1236	VSSIDUM55	0	560	1286	S768	-700	560
1237	VSSIDUM56	-14	705	1287	S769	-714	705
1238	VSSIDUM57	-28	560	1288	S770	-728	560
1239	S721	-42	705	1289	S771	-742	705
1240	S722	-56	560	1290	S772	-756	560
1241	S723	-70	705	1291	S773	-770	705
1242	S724	-84	560	1292	S774	-784	560
1243	S725	-98	705	1293	S775	-798	705
1244	S726	-112	560	1294	S776	-812	560
1245	S727	-126	705	1295	S777	-826	705
1246	S728	-140	560	1296	S778	-840	560
1247	S729	-154	705	1297	S779	-854	705
1248	S730	-168	560	1298	S780	-868	560
1249	S731	-182	705	1299	S781	-882	705
1250	S732	-196	560	1300	S782	-896	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1301	S783	-910	705	1351	S833	-1610	705
1302	S784	-924	560	1352	S834	-1624	560
1303	S785	-938	705	1353	S835	-1638	705
1304	S786	-952	560	1354	S836	-1652	560
1305	S787	-966	705	1355	S837	-1666	705
1306	S788	-980	560	1356	S838	-1680	560
1307	S789	-994	705	1357	S839	-1694	705
1308	S790	-1008	560	1358	S840	-1708	560
1309	S791	-1022	705	1359	S841	-1722	705
1310	S792	-1036	560	1360	S842	-1736	560
1311	S793	-1050	705	1361	S843	-1750	705
1312	S794	-1064	560	1362	S844	-1764	560
1313	S795	-1078	705	1363	S845	-1778	705
1314	S796	-1092	560	1364	S846	-1792	560
1315	S797	-1106	705	1365	S847	-1806	705
1316	S798	-1120	560	1366	S848	-1820	560
1317	S799	-1134	705	1367	S849	-1834	705
1318	S800	-1148	560	1368	S850	-1848	560
1319	S801	-1162	705	1369	S851	-1862	705
1320	S802	-1176	560	1370	S852	-1876	560
1321	S803	-1190	705	1371	S853	-1890	705
1322	S804	-1204	560	1372	S854	-1904	560
1323	S805	-1218	705	1373	S855	-1918	705
1324	S806	-1232	560	1374	S856	-1932	560
1325	S807	-1246	705	1375	S857	-1946	705
1326	S808	-1260	560	1376	S858	-1960	560
1327	S809	-1274	705	1377	S859	-1974	705
1328	S810	-1288	560	1378	S860	-1988	560
1329	S811	-1302	705	1379	S861	-2002	705
1330	S812	-1316	560	1380	S862	-2016	560
1331	S813	-1330	705	1381	S863	-2030	705
1332	S814	-1344	560	1382	S864	-2044	560
1333	S815	-1358	705	1383	S865	-2058	705
1334	S816	-1372	560	1384	S866	-2072	560
1335	S817	-1386	705	1385	S867	-2086	705
1336	S818	-1400	560	1386	S868	-2100	560
1337	S819	-1414	705	1387	S869	-2114	705
1338	S820	-1428	560	1388	S870	-2128	560
1339	S821	-1442	705	1389	S871	-2142	705
1340	S822	-1456	560	1390	S872	-2156	560
1341	S823	-1470	705	1391	S873	-2170	705
1342	S824	-1484	560	1392	S874	-2184	560
1343	S825	-1498	705	1393	S875	-2198	705
1344	S826	-1512	560	1394	S876	-2212	560
1345	S827	-1526	705	1395	S877	-2226	705
1346	S828	-1540	560	1396	S878	-2240	560
1347	S829	-1554	705	1397	S879	-2254	705
1348	S830	-1568	560	1398	S880	-2268	560
1349	S831	-1582	705	1399	S881	-2282	705
1350	S832	-1596	560	1400	S882	-2296	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1401	S883	-2310	705	1451	S933	-3010	705
1402	S884	-2324	560	1452	S934	-3024	560
1403	S885	-2338	705	1453	S935	-3038	705
1404	S886	-2352	560	1454	S936	-3052	560
1405	S887	-2366	705	1455	S937	-3066	705
1406	S888	-2380	560	1456	S938	-3080	560
1407	S889	-2394	705	1457	S939	-3094	705
1408	S890	-2408	560	1458	S940	-3108	560
1409	S891	-2422	705	1459	S941	-3122	705
1410	S892	-2436	560	1460	S942	-3136	560
1411	S893	-2450	705	1461	S943	-3150	705
1412	S894	-2464	560	1462	S944	-3164	560
1413	S895	-2478	705	1463	S945	-3178	705
1414	S896	-2492	560	1464	S946	-3192	560
1415	S897	-2506	705	1465	S947	-3206	705
1416	S898	-2520	560	1466	S948	-3220	560
1417	S899	-2534	705	1467	S949	-3234	705
1418	S900	-2548	560	1468	S950	-3248	560
1419	S901	-2562	705	1469	S951	-3262	705
1420	S902	-2576	560	1470	S952	-3276	560
1421	S903	-2590	705	1471	S953	-3290	705
1422	S904	-2604	560	1472	S954	-3304	560
1423	S905	-2618	705	1473	S955	-3318	705
1424	S906	-2632	560	1474	S956	-3332	560
1425	S907	-2646	705	1475	S957	-3346	705
1426	S908	-2660	560	1476	S958	-3360	560
1427	S909	-2674	705	1477	S959	-3374	705
1428	S910	-2688	560	1478	S960	-3388	560
1429	S911	-2702	705	1479	S961	-3402	705
1430	S912	-2716	560	1480	S962	-3416	560
1431	S913	-2730	705	1481	S963	-3430	705
1432	S914	-2744	560	1482	S964	-3444	560
1433	S915	-2758	705	1483	S965	-3458	705
1434	S916	-2772	560	1484	S966	-3472	560
1435	S917	-2786	705	1485	S967	-3486	705
1436	S918	-2800	560	1486	S968	-3500	560
1437	S919	-2814	705	1487	S969	-3514	705
1438	S920	-2828	560	1488	S970	-3528	560
1439	S921	-2842	705	1489	S971	-3542	705
1440	S922	-2856	560	1490	S972	-3556	560
1441	S923	-2870	705	1491	S973	-3570	705
1442	S924	-2884	560	1492	S974	-3584	560
1443	S925	-2898	705	1493	S975	-3598	705
1444	S926	-2912	560	1494	S976	-3612	560
1445	S927	-2926	705	1495	S977	-3626	705
1446	S928	-2940	560	1496	S978	-3640	560
1447	S929	-2954	705	1497	S979	-3654	705
1448	S930	-2968	560	1498	S980	-3668	560
1449	S931	-2982	705	1499	S981	-3682	705
1450	S932	-2996	560	1500	S982	-3696	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1501	S983	-3710	705	1551	S1033	-4410	705
1502	S984	-3724	560	1552	S1034	-4424	560
1503	S985	-3738	705	1553	S1035	-4438	705
1504	S986	-3752	560	1554	S1036	-4452	560
1505	S987	-3766	705	1555	S1037	-4466	705
1506	S988	-3780	560	1556	S1038	-4480	560
1507	S989	-3794	705	1557	S1039	-4494	705
1508	S990	-3808	560	1558	S1040	-4508	560
1509	S991	-3822	705	1559	S1041	-4522	705
1510	S992	-3836	560	1560	S1042	-4536	560
1511	S993	-3850	705	1561	S1043	-4550	705
1512	S994	-3864	560	1562	S1044	-4564	560
1513	S995	-3878	705	1563	S1045	-4578	705
1514	S996	-3892	560	1564	S1046	-4592	560
1515	S997	-3906	705	1565	S1047	-4606	705
1516	S998	-3920	560	1566	S1048	-4620	560
1517	S999	-3934	705	1567	S1049	-4634	705
1518	S1000	-3948	560	1568	S1050	-4648	560
1519	S1001	-3962	705	1569	S1051	-4662	705
1520	S1002	-3976	560	1570	S1052	-4676	560
1521	S1003	-3990	705	1571	S1053	-4690	705
1522	S1004	-4004	560	1572	S1054	-4704	560
1523	S1005	-4018	705	1573	S1055	-4718	705
1524	S1006	-4032	560	1574	S1056	-4732	560
1525	S1007	-4046	705	1575	S1057	-4746	705
1526	S1008	-4060	560	1576	S1058	-4760	560
1527	S1009	-4074	705	1577	S1059	-4774	705
1528	S1010	-4088	560	1578	S1060	-4788	560
1529	S1011	-4102	705	1579	S1061	-4802	705
1530	S1012	-4116	560	1580	S1062	-4816	560
1531	S1013	-4130	705	1581	S1063	-4830	705
1532	S1014	-4144	560	1582	S1064	-4844	560
1533	S1015	-4158	705	1583	S1065	-4858	705
1534	S1016	-4172	560	1584	S1066	-4872	560
1535	S1017	-4186	705	1585	S1067	-4886	705
1536	S1018	-4200	560	1586	S1068	-4900	560
1537	S1019	-4214	705	1587	S1069	-4914	705
1538	S1020	-4228	560	1588	S1070	-4928	560
1539	S1021	-4242	705	1589	S1071	-4942	705
1540	S1022	-4256	560	1590	S1072	-4956	560
1541	S1023	-4270	705	1591	S1073	-4970	705
1542	S1024	-4284	560	1592	S1074	-4984	560
1543	S1025	-4298	705	1593	S1075	-4998	705
1544	S1026	-4312	560	1594	S1076	-5012	560
1545	S1027	-4326	705	1595	S1077	-5026	705
1546	S1028	-4340	560	1596	S1078	-5040	560
1547	S1029	-4354	705	1597	S1079	-5054	705
1548	S1030	-4368	560	1598	S1080	-5068	560
1549	S1031	-4382	705	1599	S1081	-5082	705
1550	S1032	-4396	560	1600	S1082	-5096	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1601	S1083	-5110	705	1651	S1133	-5810	705
1602	S1084	-5124	560	1652	S1134	-5824	560
1603	S1085	-5138	705	1653	S1135	-5838	705
1604	S1086	-5152	560	1654	S1136	-5852	560
1605	S1087	-5166	705	1655	S1137	-5866	705
1606	S1088	-5180	560	1656	S1138	-5880	560
1607	S1089	-5194	705	1657	S1139	-5894	705
1608	S1090	-5208	560	1658	S1140	-5908	560
1609	S1091	-5222	705	1659	S1141	-5922	705
1610	S1092	-5236	560	1660	S1142	-5936	560
1611	S1093	-5250	705	1661	S1143	-5950	705
1612	S1094	-5264	560	1662	S1144	-5964	560
1613	S1095	-5278	705	1663	S1145	-5978	705
1614	S1096	-5292	560	1664	S1146	-5992	560
1615	S1097	-5306	705	1665	S1147	-6006	705
1616	S1098	-5320	560	1666	S1148	-6020	560
1617	S1099	-5334	705	1667	S1149	-6034	705
1618	S1100	-5348	560	1668	S1150	-6048	560
1619	S1101	-5362	705	1669	S1151	-6062	705
1620	S1102	-5376	560	1670	S1152	-6076	560
1621	S1103	-5390	705	1671	S1153	-6090	705
1622	S1104	-5404	560	1672	S1154	-6104	560
1623	S1105	-5418	705	1673	S1155	-6118	705
1624	S1106	-5432	560	1674	S1156	-6132	560
1625	S1107	-5446	705	1675	S1157	-6146	705
1626	S1108	-5460	560	1676	S1158	-6160	560
1627	S1109	-5474	705	1677	S1159	-6174	705
1628	S1110	-5488	560	1678	S1160	-6188	560
1629	S1111	-5502	705	1679	S1161	-6202	705
1630	S1112	-5516	560	1680	S1162	-6216	560
1631	S1113	-5530	705	1681	S1163	-6230	705
1632	S1114	-5544	560	1682	S1164	-6244	560
1633	S1115	-5558	705	1683	S1165	-6258	705
1634	S1116	-5572	560	1684	S1166	-6272	560
1635	S1117	-5586	705	1685	S1167	-6286	705
1636	S1118	-5600	560	1686	S1168	-6300	560
1637	S1119	-5614	705	1687	S1169	-6314	705
1638	S1120	-5628	560	1688	S1170	-6328	560
1639	S1121	-5642	705	1689	S1171	-6342	705
1640	S1122	-5656	560	1690	S1172	-6356	560
1641	S1123	-5670	705	1691	S1173	-6370	705
1642	S1124	-5684	560	1692	S1174	-6384	560
1643	S1125	-5698	705	1693	S1175	-6398	705
1644	S1126	-5712	560	1694	S1176	-6412	560
1645	S1127	-5726	705	1695	S1177	-6426	705
1646	S1128	-5740	560	1696	S1178	-6440	560
1647	S1129	-5754	705	1697	S1179	-6454	705
1648	S1130	-5768	560	1698	S1180	-6468	560
1649	S1131	-5782	705	1699	S1181	-6482	705
1650	S1132	-5796	560	1700	S1182	-6496	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1701	S1183	-6510	705	1751	S1233	-7210	705
1702	S1184	-6524	560	1752	S1234	-7224	560
1703	S1185	-6538	705	1753	S1235	-7238	705
1704	S1186	-6552	560	1754	S1236	-7252	560
1705	S1187	-6566	705	1755	S1237	-7266	705
1706	S1188	-6580	560	1756	S1238	-7280	560
1707	S1189	-6594	705	1757	S1239	-7294	705
1708	S1190	-6608	560	1758	S1240	-7308	560
1709	S1191	-6622	705	1759	S1241	-7322	705
1710	S1192	-6636	560	1760	S1242	-7336	560
1711	S1193	-6650	705	1761	S1243	-7350	705
1712	S1194	-6664	560	1762	S1244	-7364	560
1713	S1195	-6678	705	1763	S1245	-7378	705
1714	S1196	-6692	560	1764	S1246	-7392	560
1715	S1197	-6706	705	1765	S1247	-7406	705
1716	S1198	-6720	560	1766	S1248	-7420	560
1717	S1199	-6734	705	1767	S1249	-7434	705
1718	S1200	-6748	560	1768	S1250	-7448	560
1719	S1201	-6762	705	1769	S1251	-7462	705
1720	S1202	-6776	560	1770	S1252	-7476	560
1721	S1203	-6790	705	1771	S1253	-7490	705
1722	S1204	-6804	560	1772	S1254	-7504	560
1723	S1205	-6818	705	1773	S1255	-7518	705
1724	S1206	-6832	560	1774	S1256	-7532	560
1725	S1207	-6846	705	1775	S1257	-7546	705
1726	S1208	-6860	560	1776	S1258	-7560	560
1727	S1209	-6874	705	1777	S1259	-7574	705
1728	S1210	-6888	560	1778	S1260	-7588	560
1729	S1211	-6902	705	1779	S1261	-7602	705
1730	S1212	-6916	560	1780	S1262	-7616	560
1731	S1213	-6930	705	1781	S1263	-7630	705
1732	S1214	-6944	560	1782	S1264	-7644	560
1733	S1215	-6958	705	1783	S1265	-7658	705
1734	S1216	-6972	560	1784	S1266	-7672	560
1735	S1217	-6986	705	1785	S1267	-7686	705
1736	S1218	-7000	560	1786	S1268	-7700	560
1737	S1219	-7014	705	1787	S1269	-7714	705
1738	S1220	-7028	560	1788	S1270	-7728	560
1739	S1221	-7042	705	1789	S1271	-7742	705
1740	S1222	-7056	560	1790	S1272	-7756	560
1741	S1223	-7070	705	1791	S1273	-7770	705
1742	S1224	-7084	560	1792	S1274	-7784	560
1743	S1225	-7098	705	1793	S1275	-7798	705
1744	S1226	-7112	560	1794	S1276	-7812	560
1745	S1227	-7126	705	1795	S1277	-7826	705
1746	S1228	-7140	560	1796	S1278	-7840	560
1747	S1229	-7154	705	1797	S1279	-7854	705
1748	S1230	-7168	560	1798	S1280	-7868	560
1749	S1231	-7182	705	1799	S1281	-7882	705
1750	S1232	-7196	560	1800	S1282	-7896	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1801	S1283	-7910	705	1851	S1333	-8610	705
1802	S1284	-7924	560	1852	S1334	-8624	560
1803	S1285	-7938	705	1853	S1335	-8638	705
1804	S1286	-7952	560	1854	S1336	-8652	560
1805	S1287	-7966	705	1855	S1337	-8666	705
1806	S1288	-7980	560	1856	S1338	-8680	560
1807	S1289	-7994	705	1857	S1339	-8694	705
1808	S1290	-8008	560	1858	S1340	-8708	560
1809	S1291	-8022	705	1859	S1341	-8722	705
1810	S1292	-8036	560	1860	S1342	-8736	560
1811	S1293	-8050	705	1861	S1343	-8750	705
1812	S1294	-8064	560	1862	S1344	-8764	560
1813	S1295	-8078	705	1863	S1345	-8778	705
1814	S1296	-8092	560	1864	S1346	-8792	560
1815	S1297	-8106	705	1865	S1347	-8806	705
1816	S1298	-8120	560	1866	S1348	-8820	560
1817	S1299	-8134	705	1867	S1349	-8834	705
1818	S1300	-8148	560	1868	S1350	-8848	560
1819	S1301	-8162	705	1869	S1351	-8862	705
1820	S1302	-8176	560	1870	S1352	-8876	560
1821	S1303	-8190	705	1871	S1353	-8890	705
1822	S1304	-8204	560	1872	S1354	-8904	560
1823	S1305	-8218	705	1873	S1355	-8918	705
1824	S1306	-8232	560	1874	S1356	-8932	560
1825	S1307	-8246	705	1875	S1357	-8946	705
1826	S1308	-8260	560	1876	S1358	-8960	560
1827	S1309	-8274	705	1877	S1359	-8974	705
1828	S1310	-8288	560	1878	S1360	-8988	560
1829	S1311	-8302	705	1879	S1361	-9002	705
1830	S1312	-8316	560	1880	S1362	-9016	560
1831	S1313	-8330	705	1881	S1363	-9030	705
1832	S1314	-8344	560	1882	S1364	-9044	560
1833	S1315	-8358	705	1883	S1365	-9058	705
1834	S1316	-8372	560	1884	S1366	-9072	560
1835	S1317	-8386	705	1885	S1367	-9086	705
1836	S1318	-8400	560	1886	S1368	-9100	560
1837	S1319	-8414	705	1887	S1369	-9114	705
1838	S1320	-8428	560	1888	S1370	-9128	560
1839	S1321	-8442	705	1889	S1371	-9142	705
1840	S1322	-8456	560	1890	S1372	-9156	560
1841	S1323	-8470	705	1891	S1373	-9170	705
1842	S1324	-8484	560	1892	S1374	-9184	560
1843	S1325	-8498	705	1893	S1375	-9198	705
1844	S1326	-8512	560	1894	S1376	-9212	560
1845	S1327	-8526	705	1895	S1377	-9226	705
1846	S1328	-8540	560	1896	S1378	-9240	560
1847	S1329	-8554	705	1897	S1379	-9254	705
1848	S1330	-8568	560	1898	S1380	-9268	560
1849	S1331	-8582	705	1899	S1381	-9282	705
1850	S1332	-8596	560	1900	S1382	-9296	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1901	S1383	-9310	705	1951	S1433	-10010	705
1902	S1384	-9324	560	1952	S1434	-10024	560
1903	S1385	-9338	705	1953	S1435	-10038	705
1904	S1386	-9352	560	1954	S1436	-10052	560
1905	S1387	-9366	705	1955	S1437	-10066	705
1906	S1388	-9380	560	1956	S1438	-10080	560
1907	S1389	-9394	705	1957	S1439	-10094	705
1908	S1390	-9408	560	1958	S1440	-10108	560
1909	S1391	-9422	705	1959	SDUM2	-10122	705
1910	S1392	-9436	560	1960	SDUM3	-10136	560
1911	S1393	-9450	705	1961	VSSIDUM58	-10150	705
1912	S1394	-9464	560	1962	VSSIDUM59	-10164	560
1913	S1395	-9478	705	1963	VGLO	-10178	705
1914	S1396	-9492	560	1964	VGLO	-10192	560
1915	S1397	-9506	705	1965	VGLO	-10206	705
1916	S1398	-9520	560	1966	VGLO	-10220	560
1917	S1399	-9534	705	1967	VGLO	-10234	705
1918	S1400	-9548	560	1968	VGLO	-10248	560
1919	S1401	-9562	705	1969	VGLO	-10262	705
1920	S1402	-9576	560	1970	VGLO	-10276	560
1921	S1403	-9590	705	1971	VGLO	-10290	705
1922	S1404	-9604	560	1972	VGHO	-10304	560
1923	S1405	-9618	705	1973	VGHO	-10318	705
1924	S1406	-9632	560	1974	VGHO	-10332	560
1925	S1407	-9646	705	1975	VGHO	-10346	705
1926	S1408	-9660	560	1976	VGHO	-10360	560
1927	S1409	-9674	705	1977	VGHO	-10374	705
1928	S1410	-9688	560	1978	VGHO	-10388	560
1929	S1411	-9702	705	1979	VGHO	-10402	705
1930	S1412	-9716	560	1980	VSSIDUM60	-10416	560
1931	S1413	-9730	705	1981	VSSIDUM61	-10430	705
1932	S1414	-9744	560	1982	VSSIDUM62	-10444	560
1933	S1415	-9758	705	1983	VSSIDUM63	-10458	705
1934	S1416	-9772	560	1984	VSSIDUM64	-10472	560
1935	S1417	-9786	705	1985	VSSIDUM65	-10486	705
1936	S1418	-9800	560	1986	VSSIDUM66	-10500	560
1937	S1419	-9814	705	1987	VSSIDUM67	-10514	705
1938	S1420	-9828	560	1988	VSSIDUM68	-10528	560
1939	S1421	-9842	705	1989	VSSIDUM69	-10542	705
1940	S1422	-9856	560	1990	VSSIDUM70	-10556	560
1941	S1423	-9870	705	1991	VSSIDUM71	-10570	705
1942	S1424	-9884	560	1992	VSSIDUM72	-10584	560
1943	S1425	-9898	705	1993	VSSIDUM73	-10598	705
1944	S1426	-9912	560	1994	VSSIDUM74	-10612	560
1945	S1427	-9926	705	1995	VSSIDUM75	-10626	705
1946	S1428	-9940	560	1996	VSSIDUM76	-10640	560
1947	S1429	-9954	705	1997	VSSIDUM77	-10654	705
1948	S1430	-9968	560	1998	VSSIDUM78	-10668	560
1949	S1431	-9982	705	1999	VSSIDUM79	-10682	705
1950	S1432	-9996	560	2000	VSSIDUM80	-10696	560

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
2001	VSSIDUM81	-10710	705	2041	GOUT25	-11270	705
2002	VSSIDUM82	-10724	560	2042	GOUT26	-11284	560
2003	VSSIDUM83	-10738	705	2043	GOUT26	-11298	705
2004	VSSIDUM84	-10752	560	2044	GOUT27	-11312	560
2005	VSSIDUM85	-10766	705	2045	GOUT27	-11326	705
2006	VSSIDUM86	-10780	560	2046	GOUT28	-11340	560
2007	VSSIDUM87	-10794	705	2047	GOUT28	-11354	705
2008	VSSIDUM88	-10808	560	2048	GOUT29	-11368	560
2009	VSSIDUM89	-10822	705	2049	GOUT29	-11382	705
2010	VSSIDUM90	-10836	560	2050	GOUT30	-11396	560
2011	VSSIDUM91	-10850	705	2051	GOUT30	-11410	705
2012	VSSIDUM92	-10864	560	2052	VGLO	-11424	560
2013	VSSIDUM93	-10878	705	2053	VGLO	-11438	705
2014	VSSIDUM94	-10892	560	2054	VGLO	-11452	560
2015	VSSIDUM95	-10906	705	2055	VRGH	-11466	705
2016	VSSIDUM96	-10920	560	2056	VRGH	-11480	560
2017	VSSIDUM97	-10934	705	2057	VRGH	-11494	705
2018	VSSIDUM98	-10948	560	2058	LVGL	-11508	560
2019	VSSIDUM99	-10962	705	2059	LVGL	-11522	705
2020	VSSIDUM100	-10976	560	2060	LVGL	-11536	560
2021	VSSIDUM101	-10990	705	2061	GOUT31	-11550	705
2022	VSSIDUM102	-11004	560	2062	GOUT31	-11564	560
2023	VSSIDUM103	-11018	705	2063	GOUT32	-11578	705
2024	GOUT17	-11032	560	2064	GOUT32	-11592	560
2025	GOUT17	-11046	705	2065	VGLO	-11606	705
2026	GOUT18	-11060	560	2066	VGLO	-11620	560
2027	GOUT18	-11074	705	2067	VGLO	-11634	705
2028	GOUT19	-11088	560	2068	VGHO	-11648	560
2029	GOUT19	-11102	705	2069	VGHO	-11662	705
2030	GOUT20	-11116	560	2070	VGHO	-11676	560
2031	GOUT20	-11130	705	2071	PADA4	-11690	705
2032	GOUT21	-11144	560	2072	PADB4	-11704	560
2033	GOUT21	-11158	705	2073	VSSIDUM104	-11718	705
2034	GOUT22	-11172	560	2074	VSSIDUM105	-11732	560
2035	GOUT22	-11186	705	2075	VSSIDUM106	-11760	705
2036	GOUT23	-11200	560				
2037	GOUT23	-11214	705				
2038	GOUT24	-11228	560				
2039	GOUT24	-11242	705		ALMARK_R_T	11870	687.5
2040	GOUT25	-11256	560		ALMARK_L_T	-11870	687.5

5.3 Mapping Table of Gate Control Signals

Pad No.	Pad Name	Output Signal (LR=1)	Pad No.	Pad Name	Output Signal (LR=0)
2068~2070	VGHO	VGH	2068~2070	VGHO	VGH
2065~2067	VGLO	VGL	2065~2067	VGLO	VGL
2063~2064	**GOUT32**	**BW_E**	2063~2064	**GOUT32**	**BW_O**
2061~2062	**GOUT31**	**FW_E**	2061~2062	**GOUT31**	**FW_O**
2058~2060	LVGL	LVGL	2058~2060	LVGL	LVGL
2055~2057	VRGH	VBIAS	2055~2057	VRGH	VBIAS
2052~2054	VGLO	VGL	2052~2054	VGLO	VGL
2050~2051	**GOUT30**	**CK_E**	2050~2051	**GOUT30**	**CK_O**
2048~2049	**GOUT29**	**CKB_E**	2048~2049	**GOUT29**	**CKB_O**
2046~2047	**GOUT28**	**STP_E**	2046~2047	**GOUT28**	**STP_O**
2044~2045	**GOUT27**	**BW_E**	2044~2045	**GOUT27**	**BW_O**
2042~2043	**GOUT26**	**FW_E**	2042~2043	**GOUT26**	**FW_O**
2024~2041	GOUT17~25	VGL	2024~2041	GOUT17~25	VGL
1980~2023	VSSIDUM60~103	VSSI	1980~2023	VSSIDUM60~103	VSSI
1972~1979	VGHO	VGH	1972~1979	VGHO	VGH
1963~1971	VGLO	VGL	1963~1971	VGLO	VGL
1961~1962	VSSIDUM58~59	VSSI	1961~1962	VSSIDUM58~59	VSSI
:	:	:	:	:	:
466~467	VSSIDUM8~7	VSSI	466~467	VSSIDUM8~7	VSSI
457~465	VGLO	VGL	457~465	VGLO	VGL
449~456	VGHO	VGH	449~456	VGHO	VGH
431~448	GOUT8~16	VGL	431~448	GOUT8~16	VGL
429~430	**GOUT7**	**FW_O**	429~430	**GOUT7**	**FW_E**
427~428	**GOUT6**	**BW_O**	427~428	**GOUT6**	**BW_E**
425~426	**GOUT5**	**STP_O**	425~426	**GOUT5**	**STP_E**
423~424	**GOUT4**	**CKB_O**	423~424	**GOUT4**	**CKB_E**
421~422	**GOUT3**	**CK_O**	421~422	**GOUT3**	**CK_E**
418~420	VGLO	VGL	418~420	VGLO	VGL
415~417	VRGH	VBIAS	415~417	VRGH	VBIAS
412~414	LVGL	LVGL	412~414	LVGL	LVGL
410~411	**GOUT2**	**FW_O**	410~411	**GOUT2**	**FW_E**
408~409	**GOUT1**	**BW_O**	408~409	**GOUT1**	**BW_E**
402~407	VGHO	VGH	402~407	VGHO	VGH

6 SERIAL INTERFACE FOR 4-PIN SPI (8-BIT) AND 3-PIN SPI (9-BIT)

6.1 Pin Description

6.1.1 SPI Interface Pin

Symbol	I/O	Description
CSX	I	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. This pin is not used for MIPI or MDDI I/F, please connect to VSSI this pin.
WRX / SCL / I2C_SCL	I	WRX: Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.
RDX	I	This pin is not used for 8-bit / 9-bit SPI I/F, please connect to VDDI this pin.
SDI / I2C_SDA	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal. I2C_SDA: Serial input/output signal in I2C I/F. The data is input/output on the rising edge of the I2C_SCL signal. This pin is not used for 80-series MPU or MIPI I/F, please connect to VSSI this pin.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please open this pin.

6.1.2 Interface Logic Pin

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>Interface type selection. The connections of IM[3:0] which not shown in table are invalid.
<table>
<tr><th>IM[3:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>0000</td><td>80-series 8-bit MPU I/F, D[7:0]</td><td>80-series 8-bit MPU I/F, D[7:0]</td></tr>
<tr><td>0001</td><td>80-series 16-bit MPU I/F, D[15:0]</td><td>80-series 16-bit MPU I/F, D[15:0]</td></tr>
<tr><td>0010</td><td>80-series 24-bit MPU I/F, D[23:0]</td><td>80-series 24-bit MPU I/F, D[23:0]</td></tr>
<tr><td>1001</td><td>RGB I/F, D[23:0]</td><td>8-bit SPI, SDI/SDO</td></tr>
<tr><td>1010</td><td>RGB I/F, D[23:0]</td><td>9-bit SPI, SDI/SDO</td></tr>
<tr><td>0011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>1011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0100</td><td>RGB I/F, D[23:0]</td><td>I2C I/F, I2C_SDA</td></tr>
<tr><td>0101</td><td>MIPI DSI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MIPI DSI,
HSSI_D0_P/N, HSSI_D1_P/N</td></tr>
<tr><td>0110</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>0110</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0111</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
I2C I/F, I2C_SDA serial data</td></tr>
</table>
</td></tr>
</table>

6.2 Functional Description

The 4-pin SPI (8-bit) and 3-pin SPI (9-bit) selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in ***Table 6.2.1***.

Table 6.2.1 Interface Type Selection

IM3	IM2	IM1	IM0	SRAM	Register
0	0	0	0	80-series 8-bit MPU interface, D[7:0]	80-series 8-bit MPU interface, D[7:0]
0	0	0	1	80-series 16-bit MPU interface, D[15:0]	80-series 16-bit MPU interface, D[15:0]
0	0	1	0	80-series 24-bit MPU interface, D[23:0]	80-series 24-bit MPU interface, D[23:0]
1	0	0	1	RGB interface, D[23:0]	8-bit SPI, SDI/SDO
1	0	1	0	RGB interface, D[23:0]	9-bit SPI, SDI/SDO
0	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO, SCL falling trigger
0	1	0	0	RGB interface, D[23:0]	I2C interface, I2C_SDA
0	1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N
0	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO, SCL rising trigger
1	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO, SCL falling trigger
0	1	1	1	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N I2C interface, I2C_SDA

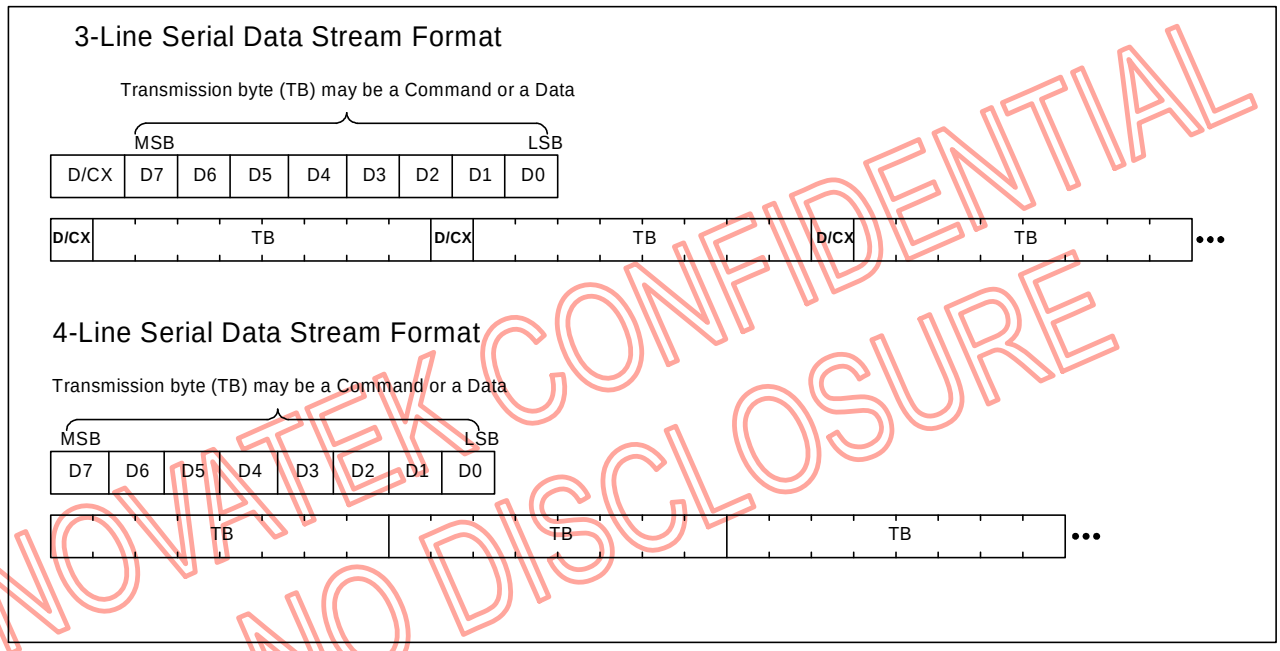
Note: "X" = Don't care.

The 3-pin SPI (9-bit format) use CSX (chip select), SCL (serial clock) and SDI/SDO (serial data input/output). The 4-pin SPI (8-bit format) use CSX (chip select), D/CX (data/command select), SCL (serial clock) and SDI/SDO (serial data input/output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

6.2.1 Write Mode

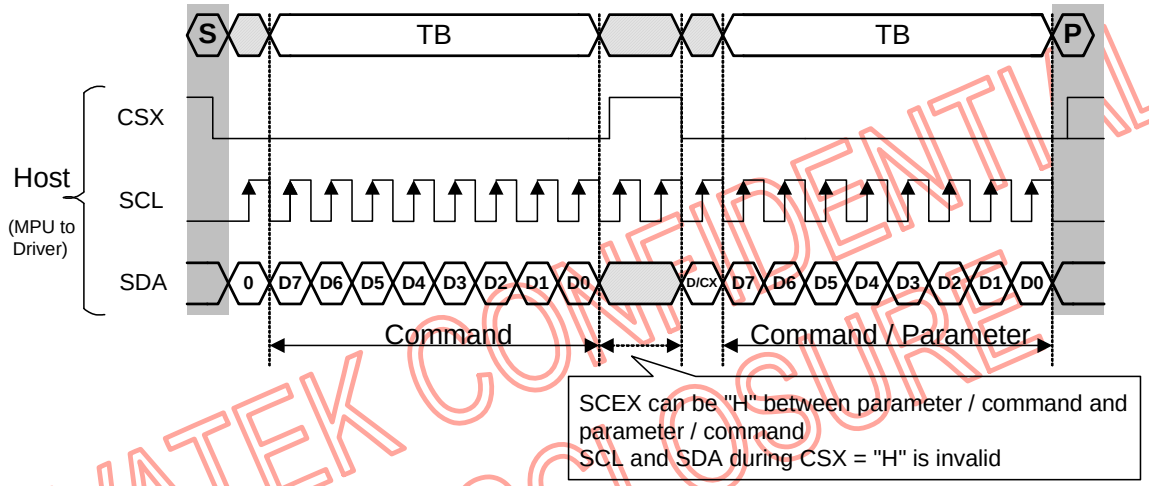
The write mode of the interface means the micro controller writes commands and data to the NT35510. 3-Pin serial data packet contains a control bit D/CX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control bit D/CX is transferred by D/CX pin. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the NT35510. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI/SDO data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

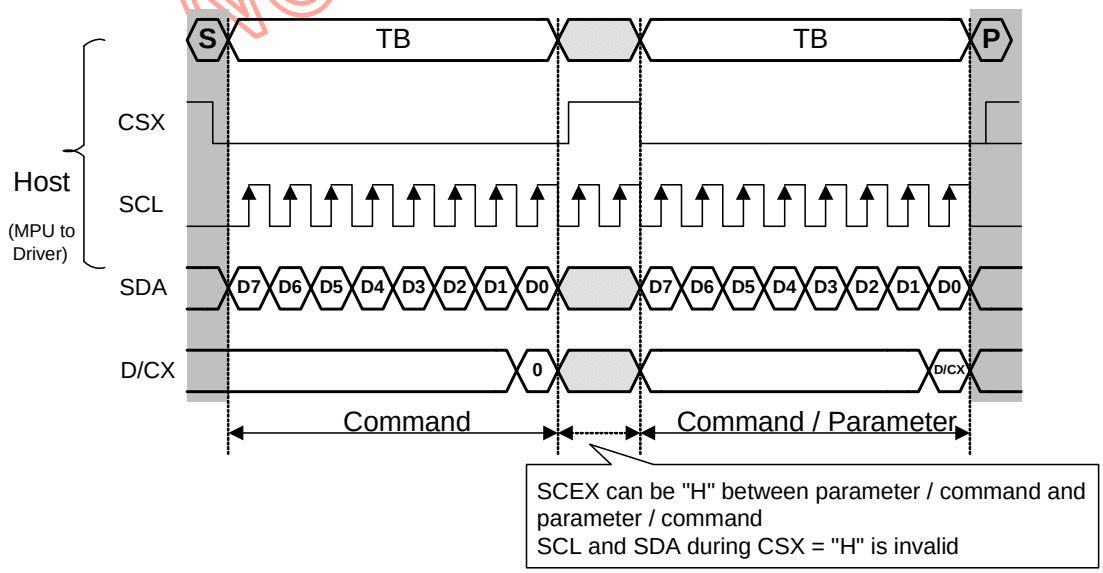


When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (see below figure). SDI/SDO is sampled at the rising edge of SCL. D/CX indicates, whether the byte is command code (D/CX=0) or parameter/RAM data (D/CX=1). It is sampled when first rising SCL edge (3-line serial interface) or 8th rising SCLK edge (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

1) 3-Pin Serial Interface Protocol for Register Write

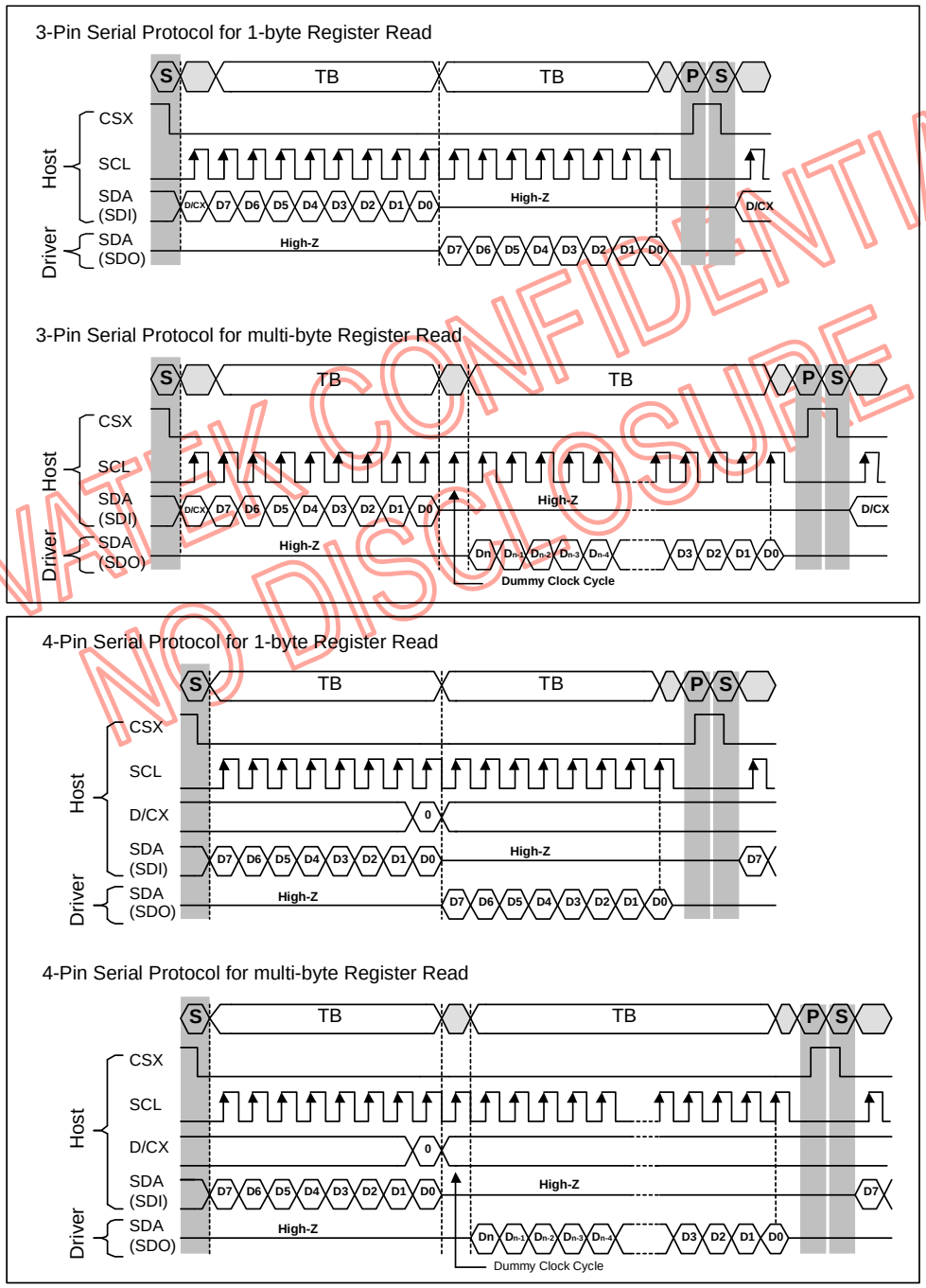


2) 4-Pin Serial Interface Protocol for Register Write



6.2.2 Read Mode

The read mode of the interface means that the micro controller reads register value from the NT35510. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The NT35510 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDO line must be set to tri-state no later than at the falling SCL edge of the last bit.



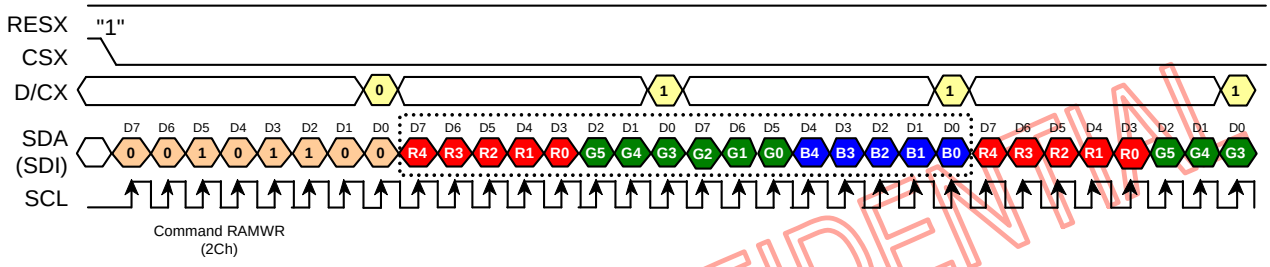
6.2.3 Data RAM Write

The 4-pin SPI (8-bit) and 3-pin SPI (9-bit) are used with RGB interface (IM[2:0]="011"). In RGB+SPI interface, the data RAM write function for SPI is valid when bit ICM="1" (command B3h of page 0). Different display data formats are available for three color depths supported by the LCM listed below:

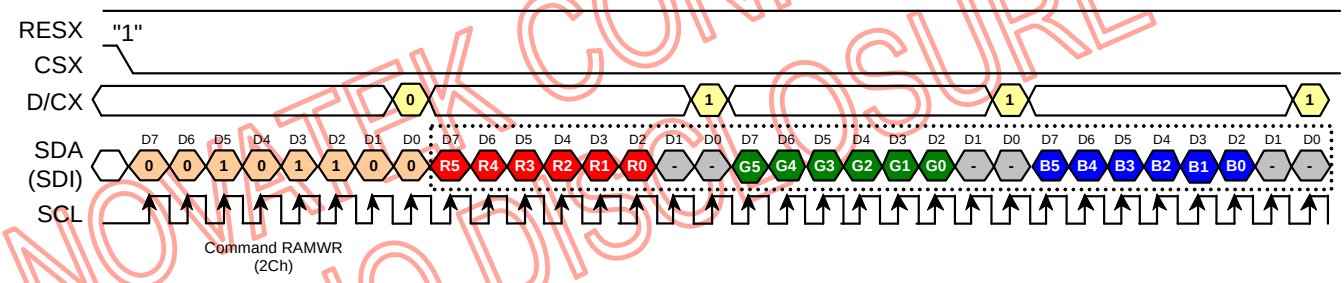
6.2.3.1 4-PIN (8-BIT) SERIAL INTERFACE

Different display data formats are available for three color depths supported by the LCM listed below:

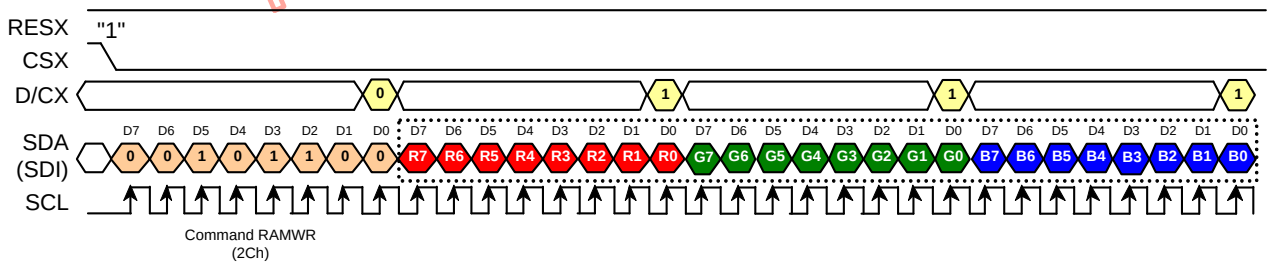
- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3Ah is 0x05)



- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3Ah is 0x06)



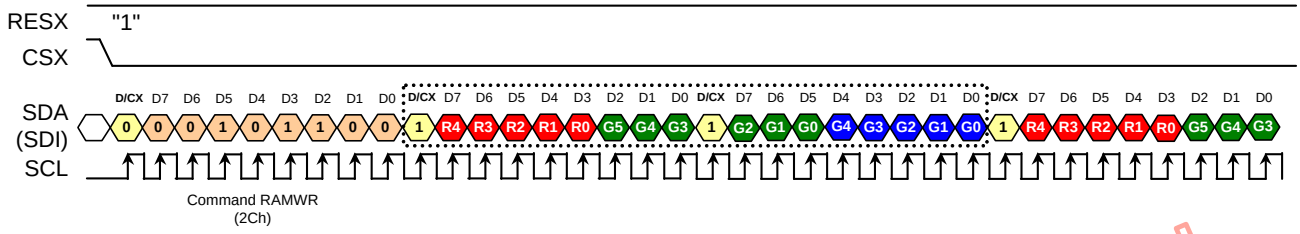
- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3Ah is 0x07)



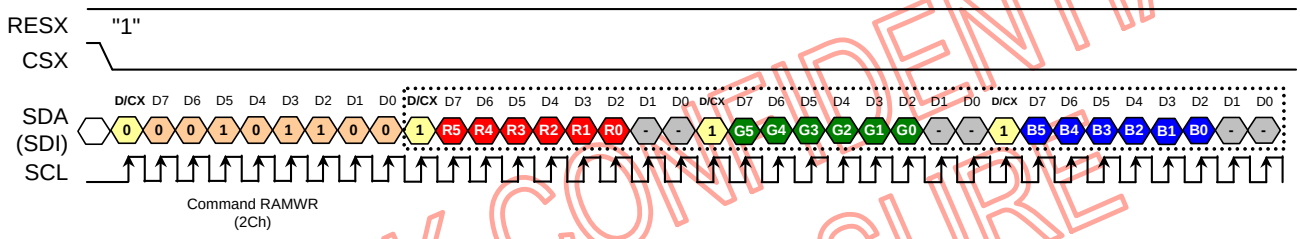
6.2.3.2 3-PIN (9-BIT) SERIAL INTERFACE

Different display data formats are available for three color depths supported by the LCM listed below:

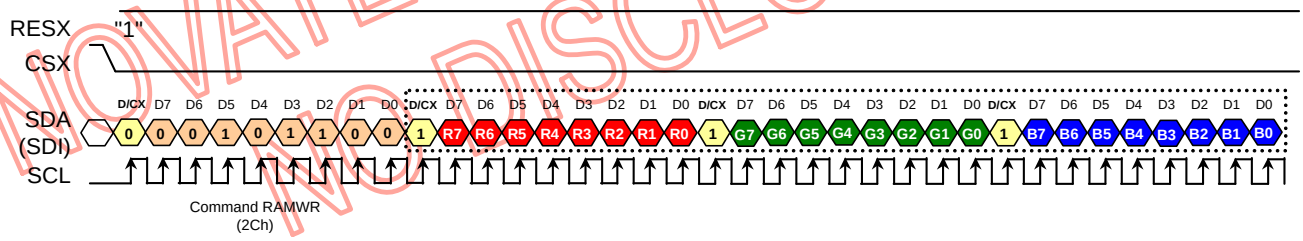
- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3Ah is 0x05)



- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3Ah is 0x06)



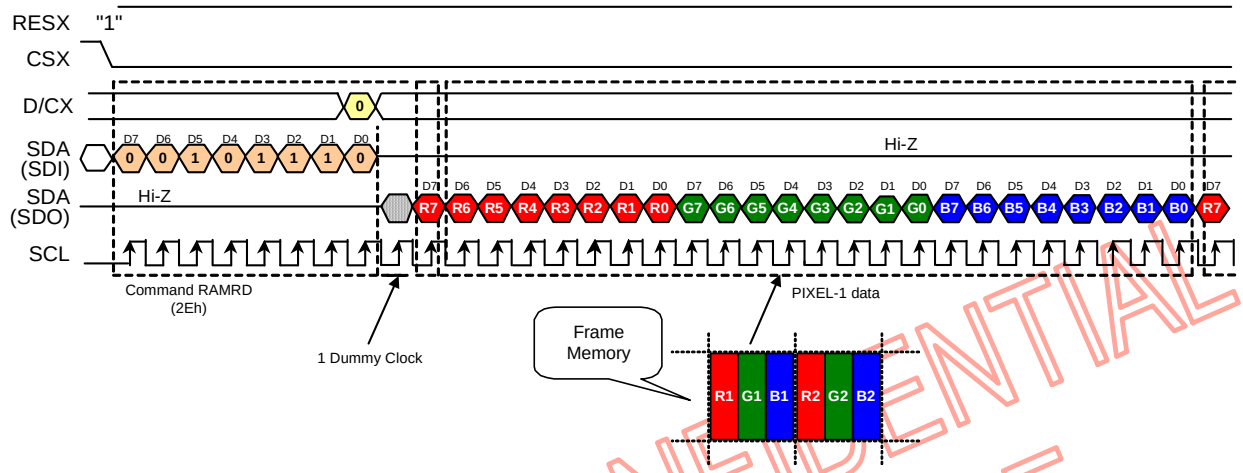
- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3Ah is 0x07)



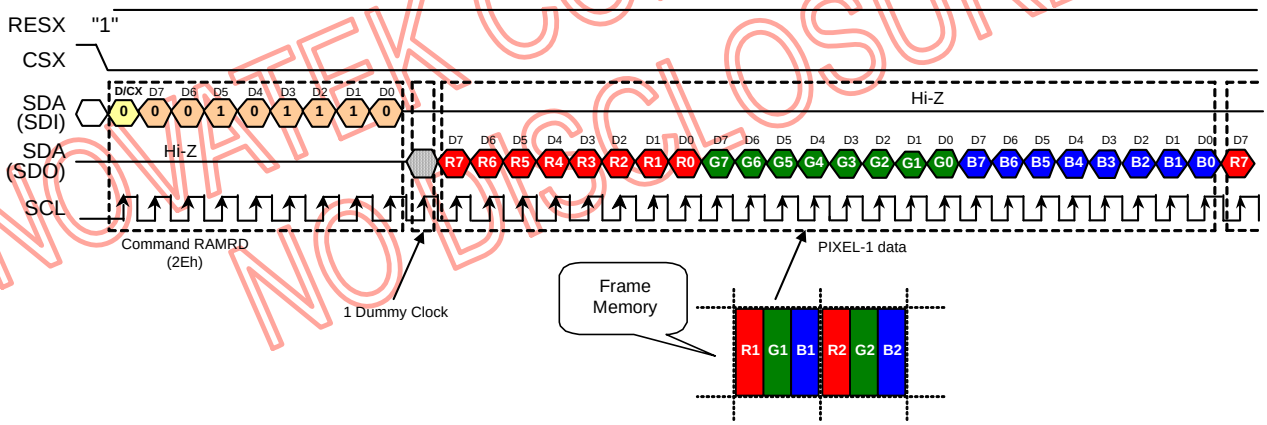
6.2.4 Data RAM Read

The read data RGB is 8-8-8-bit output as below.

- 4-pin SPI (8-bit)



- 3-pin SPI (9-bit)

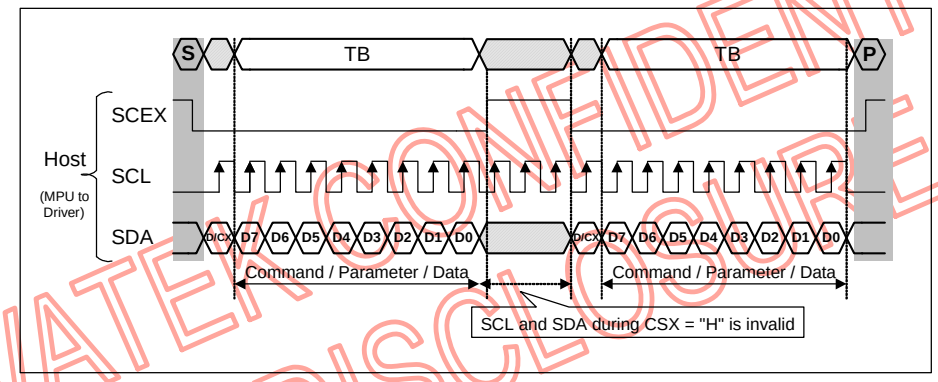


6.3 Interface Pause

By using parallel interface, it is possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the CSX (Chip Select Line) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT35510 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the CSX (Chip Select Line) is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the CSX (Chip Select Line) is next enabled as shown below.

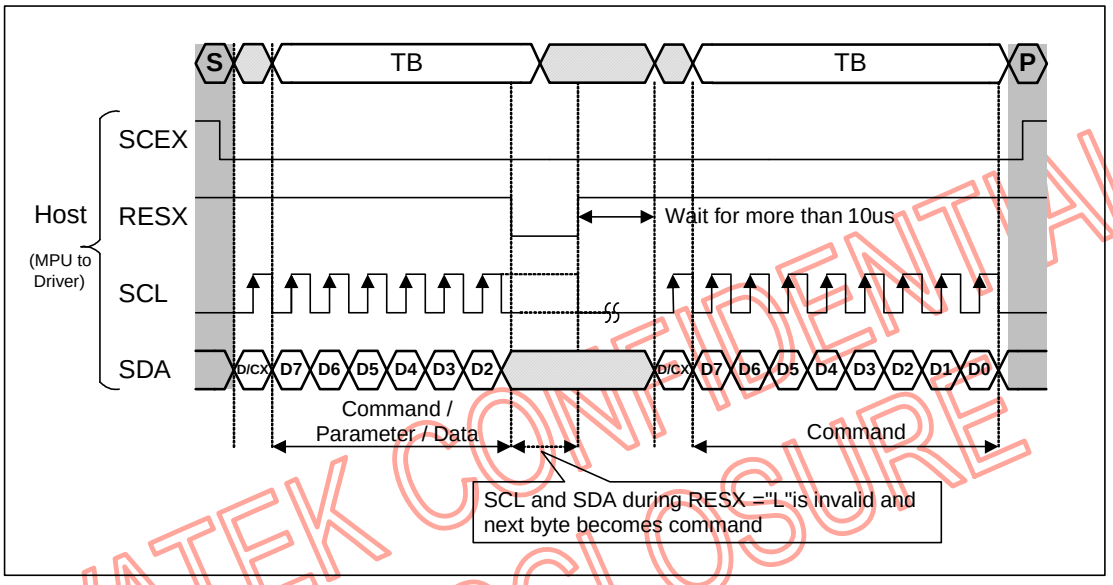
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Serial Interface Pause

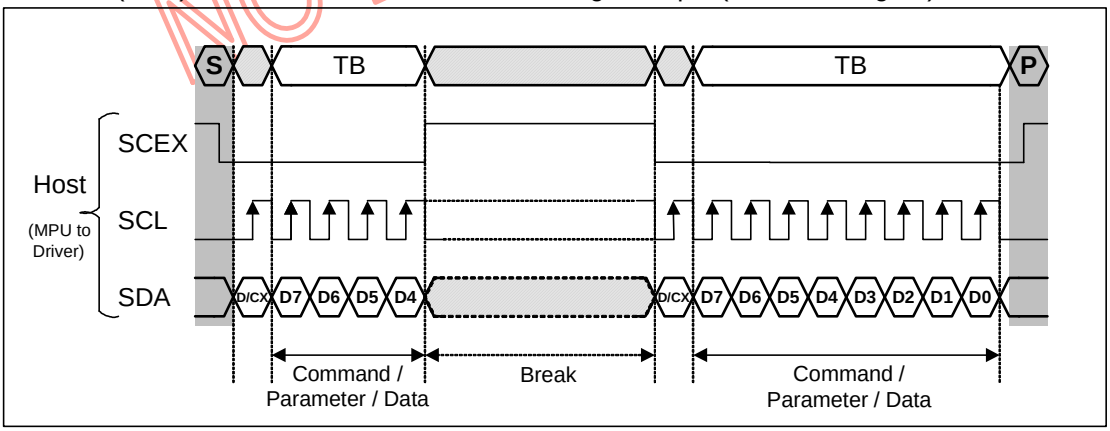


6.4 Data Transfer Break and Recovery

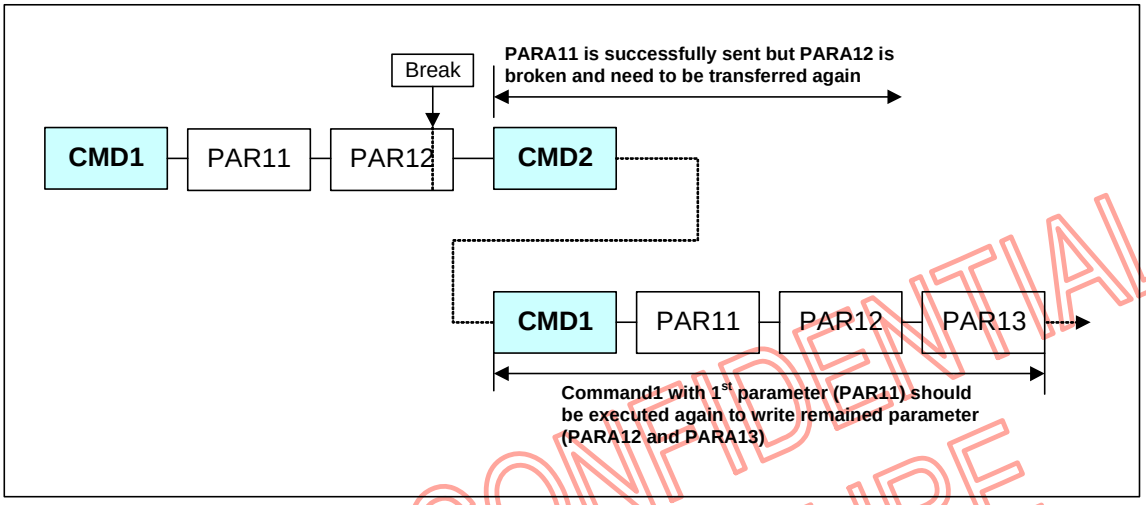
If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example (See below figure)



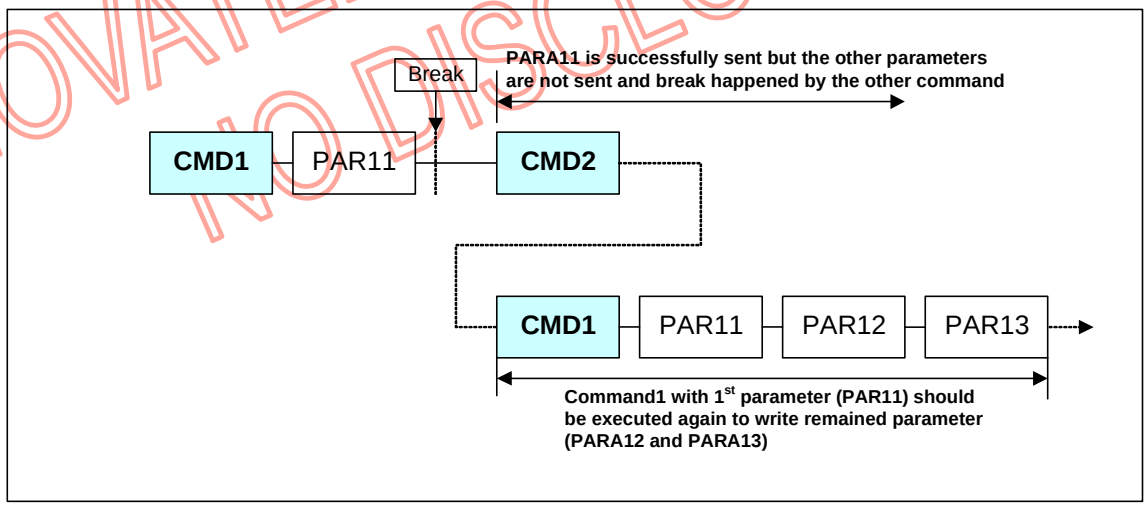
If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example (See below figure)



If 1, 2 or more parameter command is being sent and a break occure while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

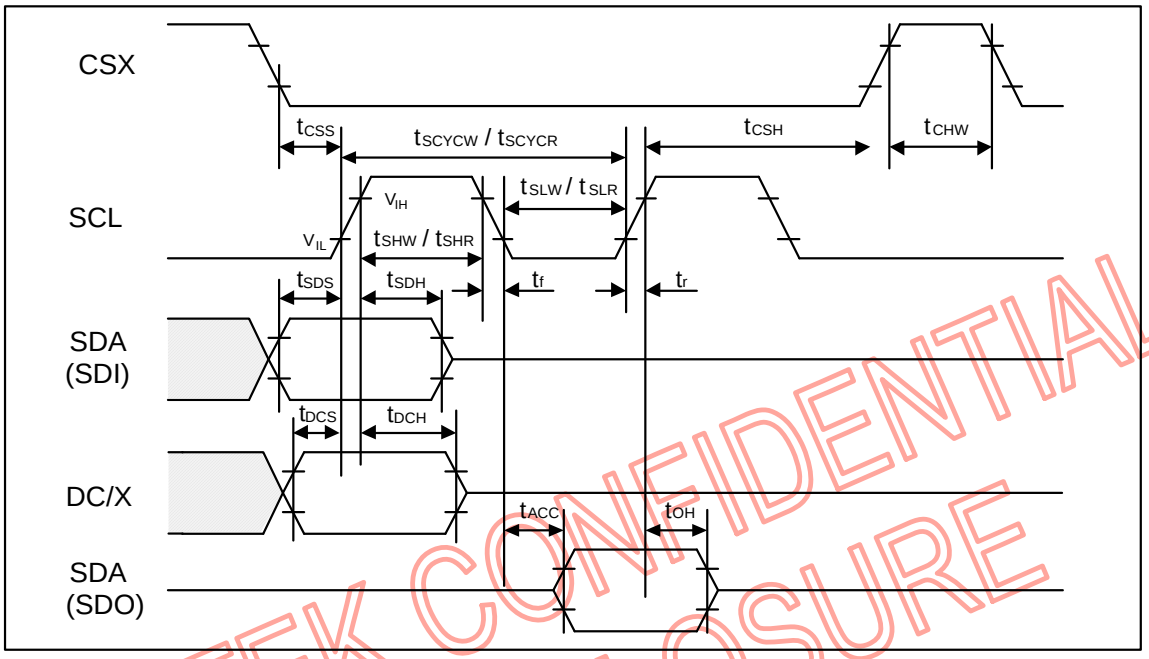


If a 2 or more parameter command is being sent and a break occure by the other command before the last one is sent, then the the parameters that were successfully sent are stored and the other parameter of that command remains previous value.



6.5 AC Characteristics

6.5.1 Serial Interface Characteristics (4-pin SPI, 8-bit)

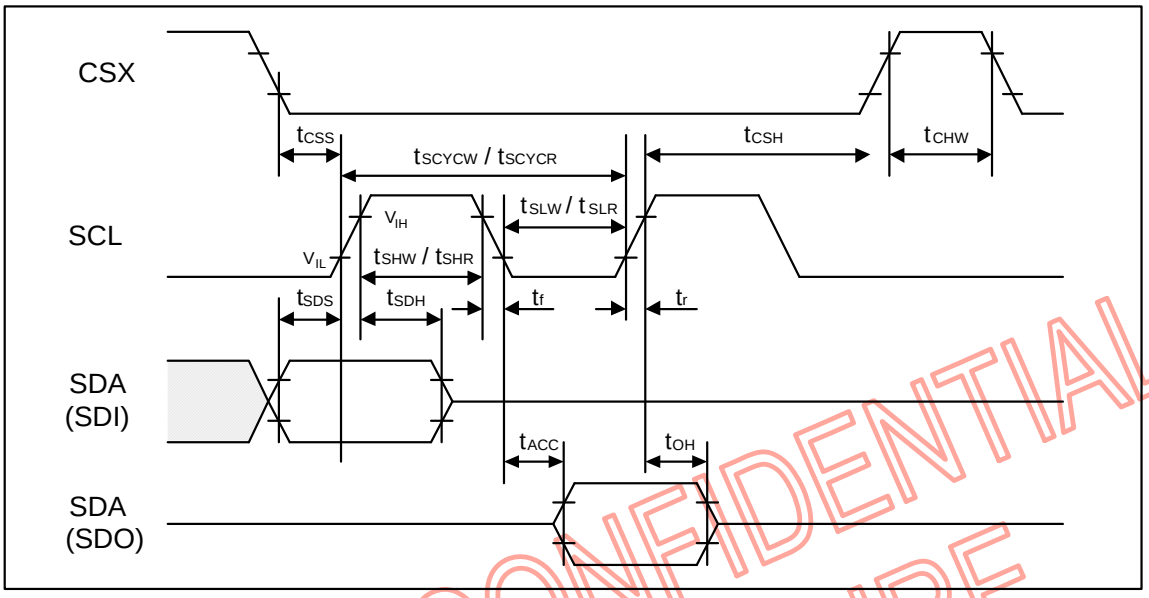


(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL "H" pulse width (Write)	30	-	ns	
	t_{SLW}	SCL "L" pulse width (Write)	30	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read GRAM)	60	-	ns	
	t_{SLR}	SCL "L" pulse width (Read GRAM)	60	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read ID)	60	-	ns	
	t_{SLR}	SCL "L" pulse width (Read ID)	60	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	20	-	ns	
	t_{SDH}	Data hold time	20	-	ns	
	t_{ACC}	Access time	10	50	ns	For maximum C_L=30pF
	t_{OH}	Output disable time	15	50	ns	For minimum C_L=8pF
D/CX	t_{DCS}	D/CX setup time	30	-	ns	
	t_{DCH}	D/CX hold time	30	-	ns	
CSX	t_{CHW}	Chip select "H" pulse width	40	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

6.5.2 Serial Interface Characteristics (3-pin SPI, 9-bit)



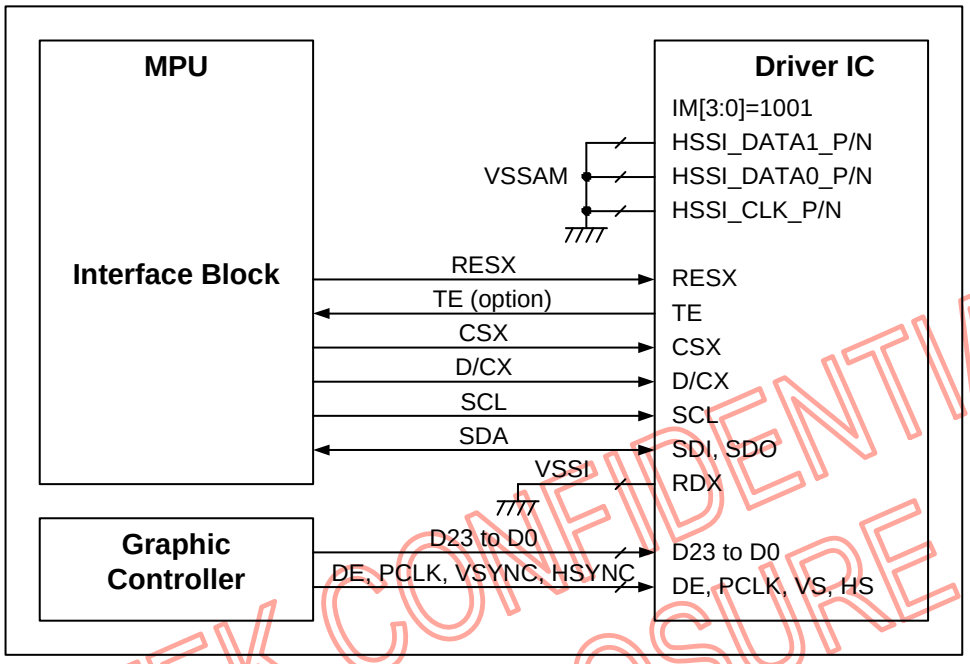
(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL "H" pulse width (Write)	30	-	ns	
	t_{SLW}	SCL "L" pulse width (Write)	30	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read GRAM)	60	-	ns	
	t_{SLR}	SCL "L" pulse width (Read GRAM)	60	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read ID)	60	-	ns	
	t_{SLR}	SCL "L" pulse width (Read ID)	60	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	20	-	ns	
	t_{SDH}	Data hold time	20	-	ns	
	t_{ACC}	Access time	10	50	ns	For maximum C_L=30pF
	t_{OH}	Output disable time	15	50	ns	For minimum C_L=8pF
CSX	t_{CHW}	Chip select "H" pulse width	40	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

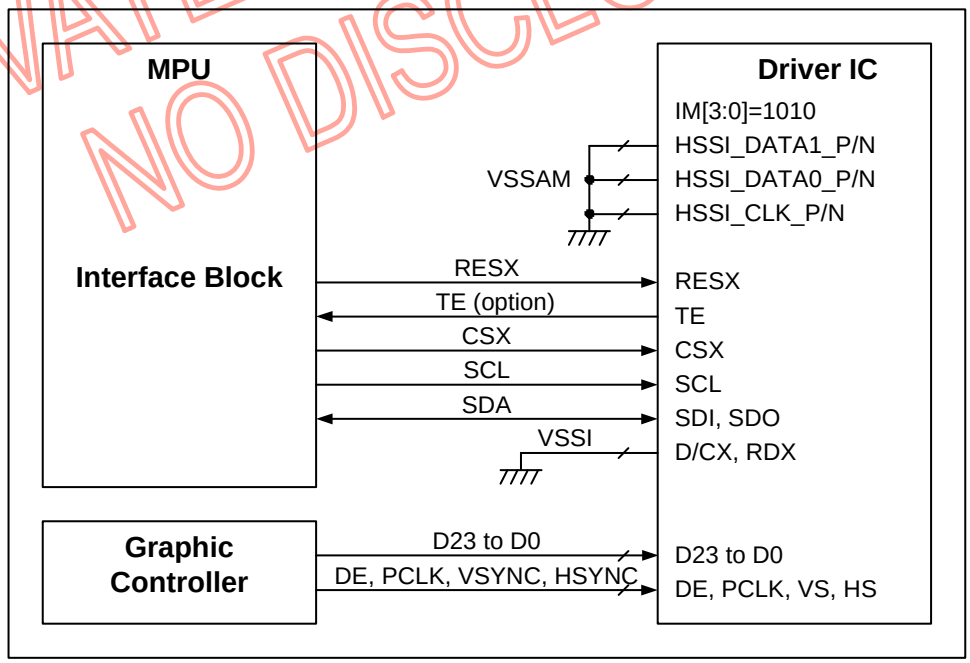
Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

6.6 Microprocessor Interface

The display, which is using RGB with 4-pin (8-bit)SPI interface, is connected to the MPU as it is illustrated below.



The display, which is using RGB with 3-pin (9-bit)SPI interface, is connected to the MPU as it is illustrated below.



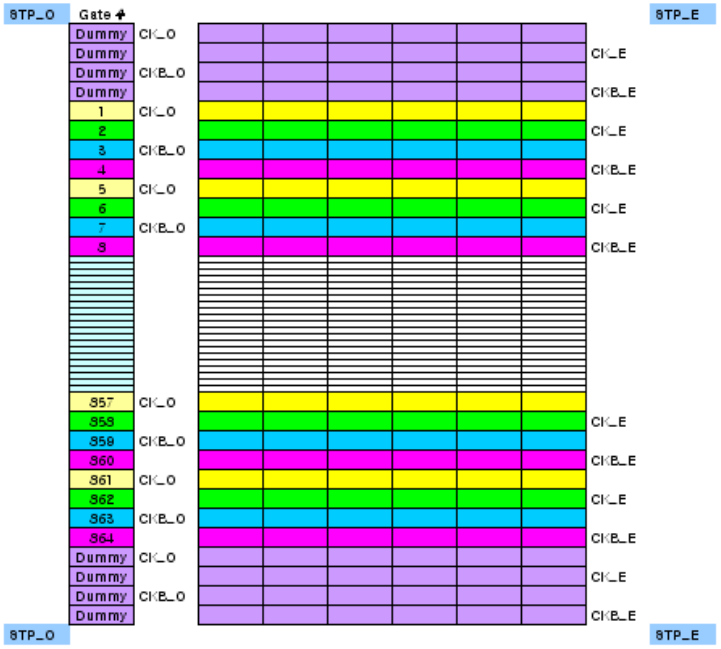
Note 1. Connecting D23, D22, D15, D14, D7 and D6 to VSSI when using 18-bit/pixel (VIPF[3:0]="0110").
Connecting D23~D21, D15, D14 and D7~ D5 to VSSI when using 16-bit/pixel (VIPF[3:0]="0101").
Note 2. Left MVDDL and MVDDA open (not used) when using RGB with SPI interface.

7 Timing Example

In this section we listed timing example for Non-overlap, Dual scan and Overlap, Dual scan. The relative setting registers are presented in Display timing control section.

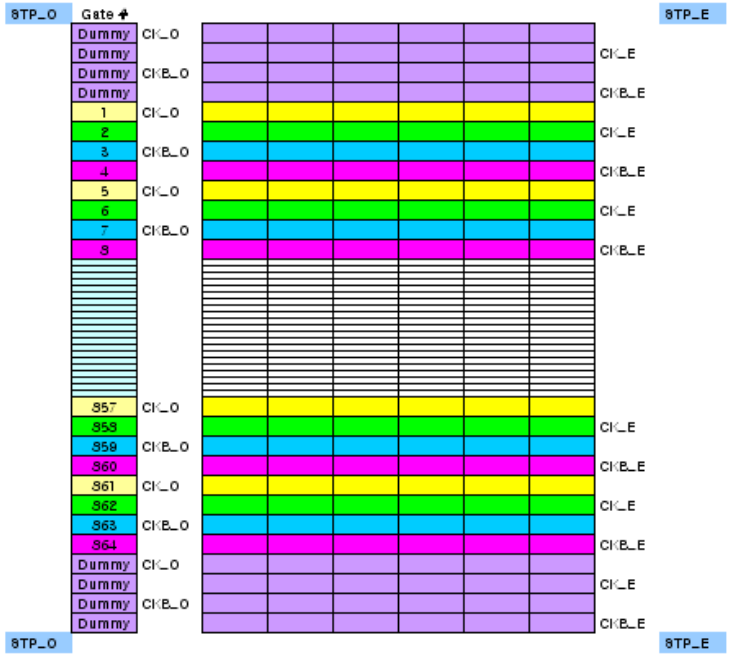
This is an example for Non-overlap, Dual Scan, 480RGBx864, Forward Scan.

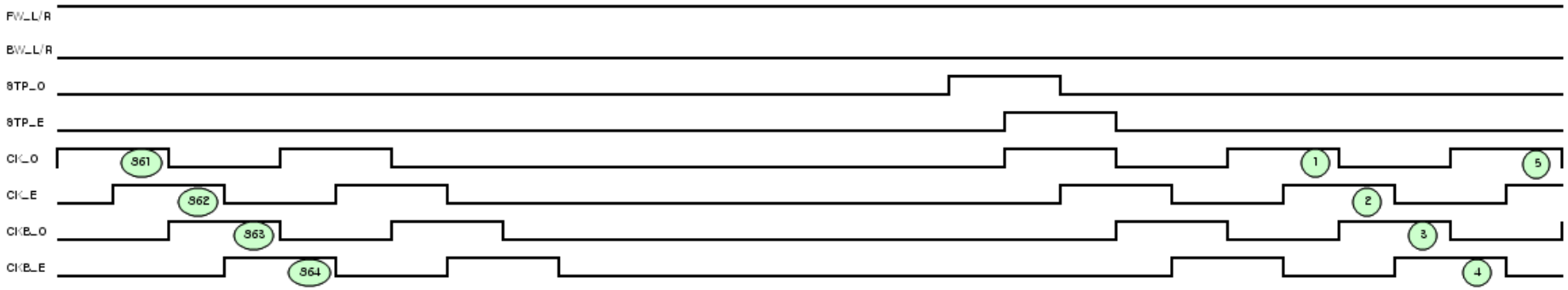
Forward Scan
Non-Overlapping



This is an example for Overlap, Dual scan, 480RGBx864, Forward Scan.

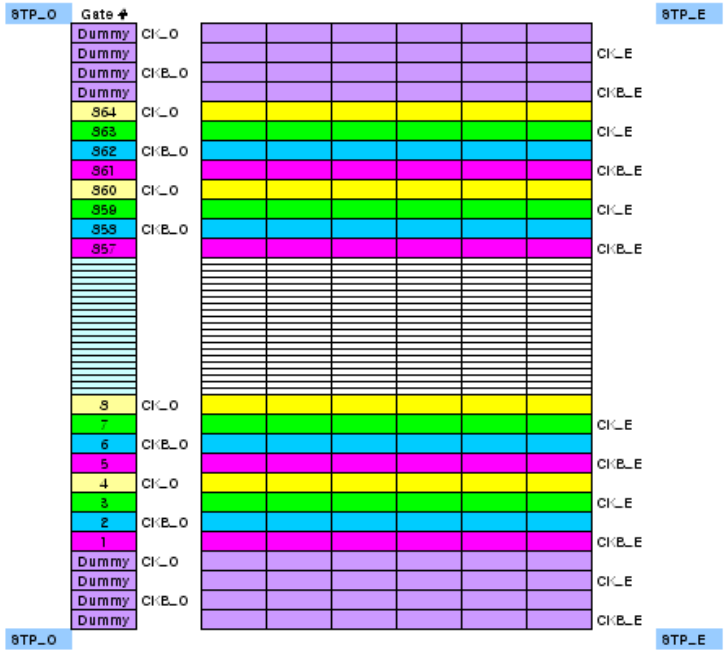
Forward Scan Overlapping

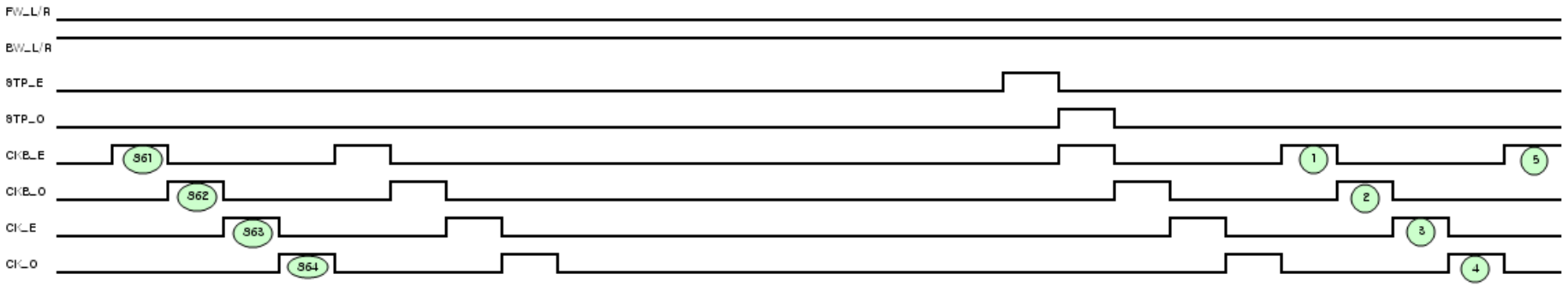




This is an example for Non-overlap, Dual scan, 480RGBx864, Backward Scan.

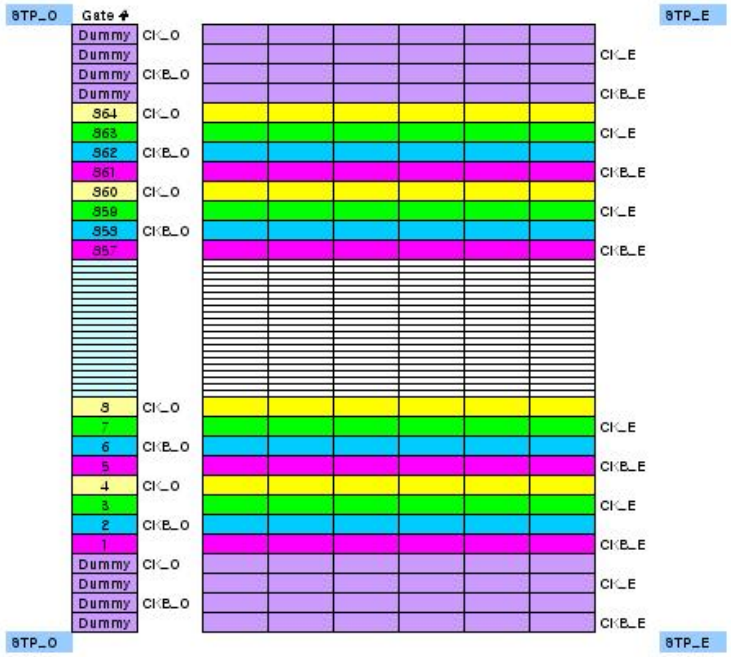
Backward Scan
Non-Overlapping

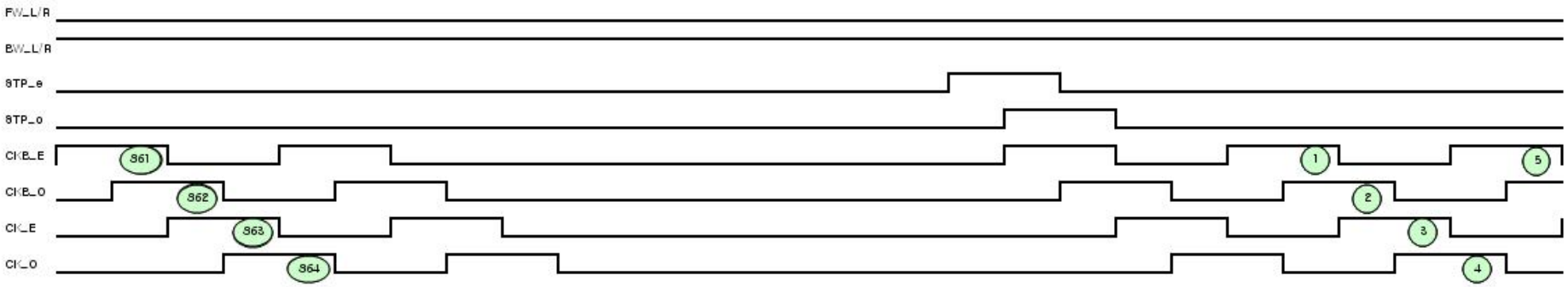




This is an example for Overlap, Dual scan, 480RGBx864, Backward Scan.

Backward Scan
Overlapping



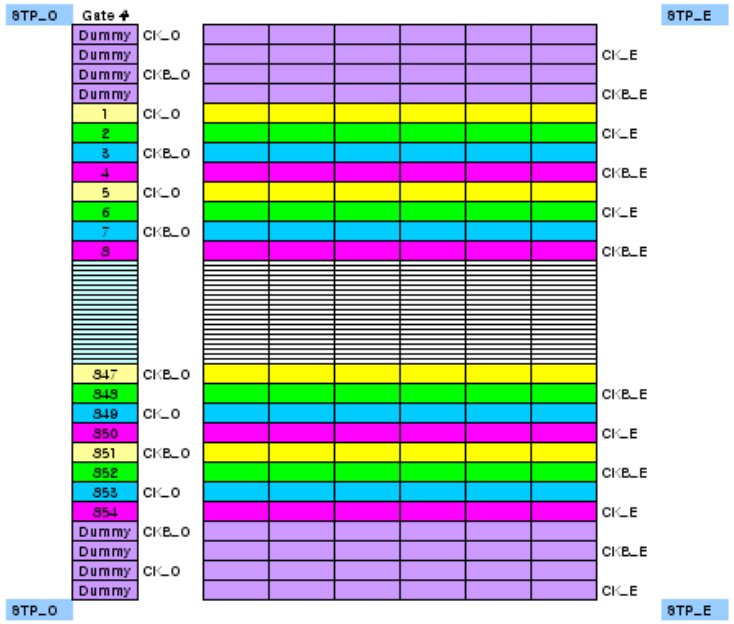


This is an example for Non-overlap, Dual scan, 480RGBx854, Forward Scan.

Forward Scan
Non-Overlapping

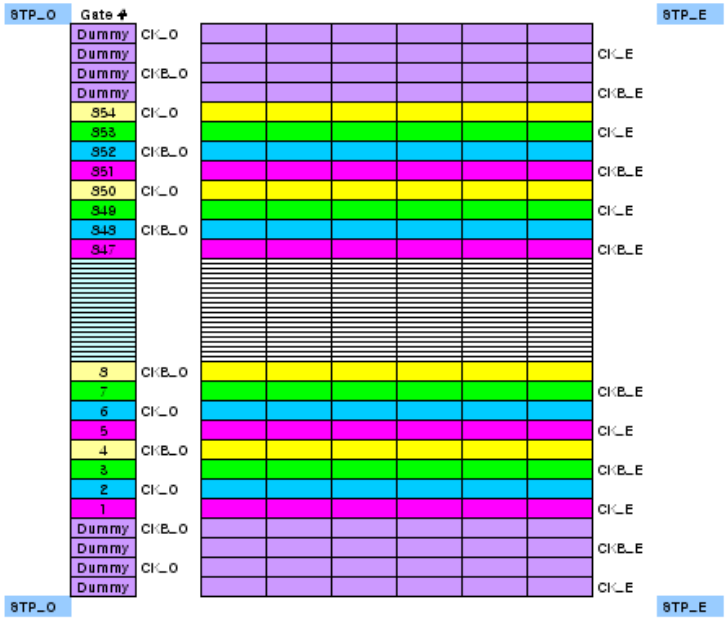
This is an example for Overlap, Dual scan, 480RGBx854, Forward Scan.

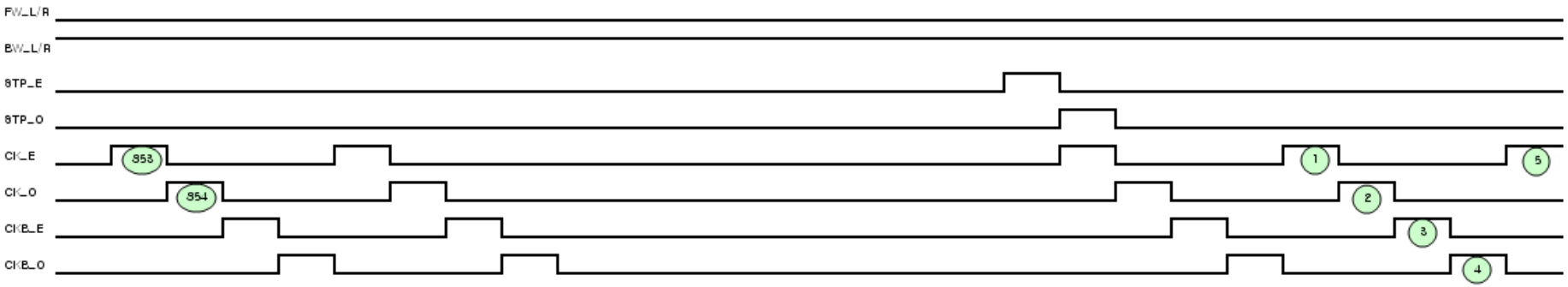
Forward Scan Overlapping



This is an example for Non-overlap, Dual scan, 480RGBx854, Backward Scan.

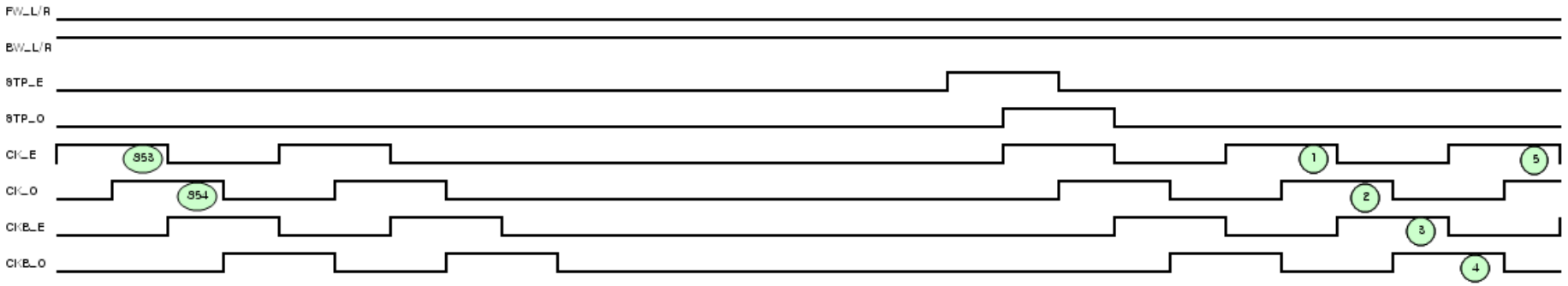
Backward Scan
Non-Overlapping





This is an example for Overlap, Dual scan, 480RGBx854, Backward Scan.

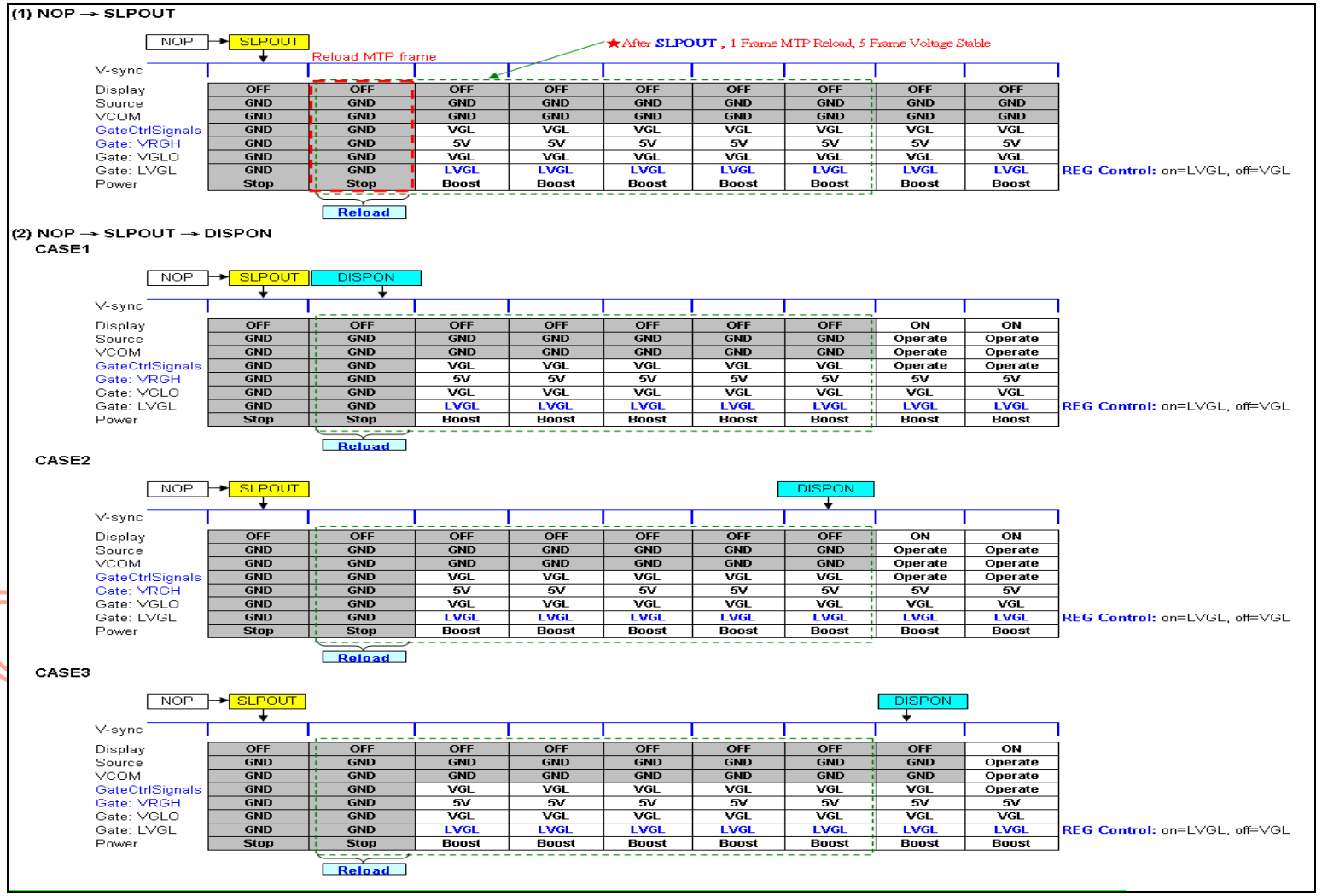
Backward Scan Overlapping



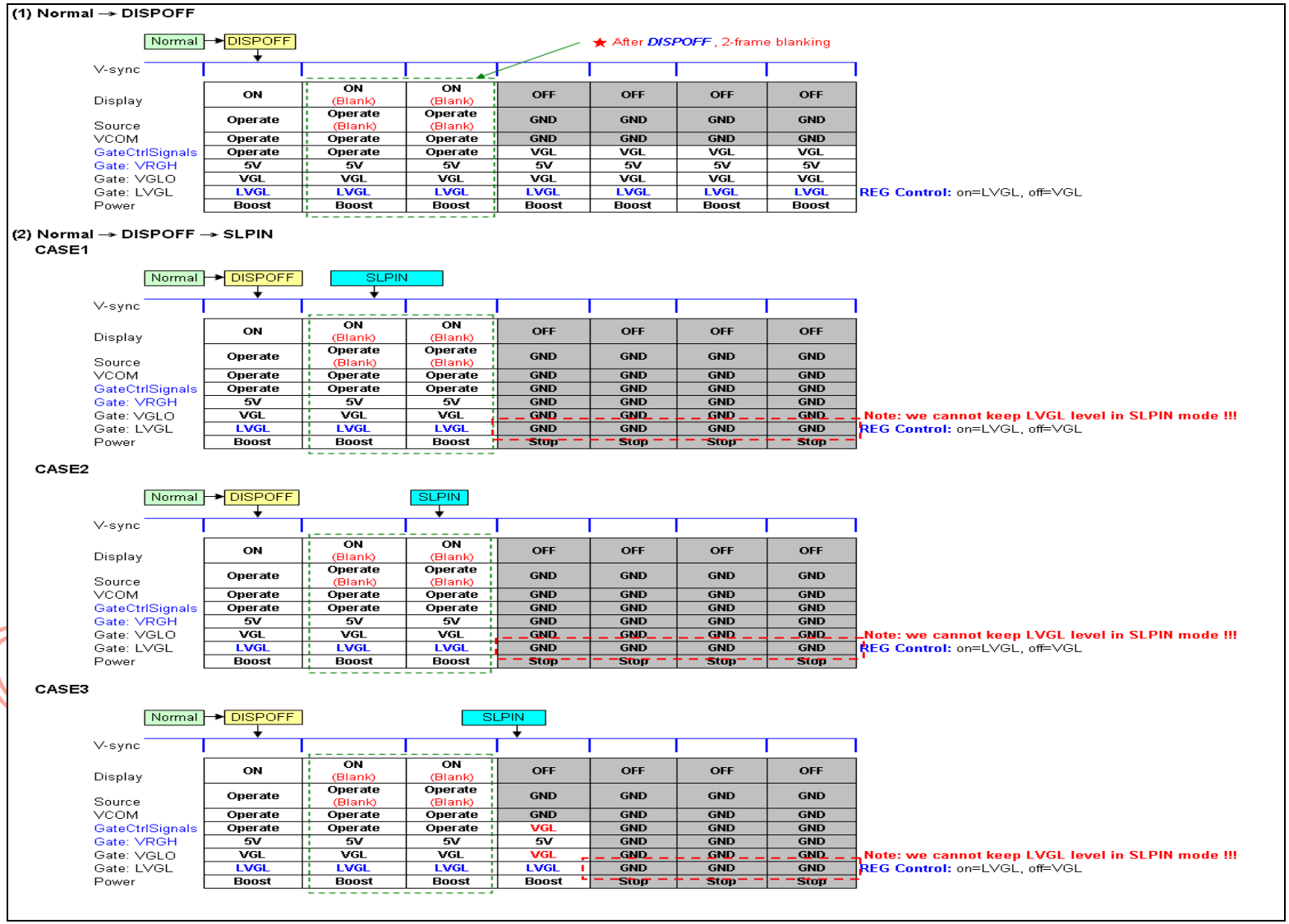
8 Auto Sequence

In this section we listed Auto sequence to present the status of DIC in each frame for Power On/Off, and Abnormal power off.

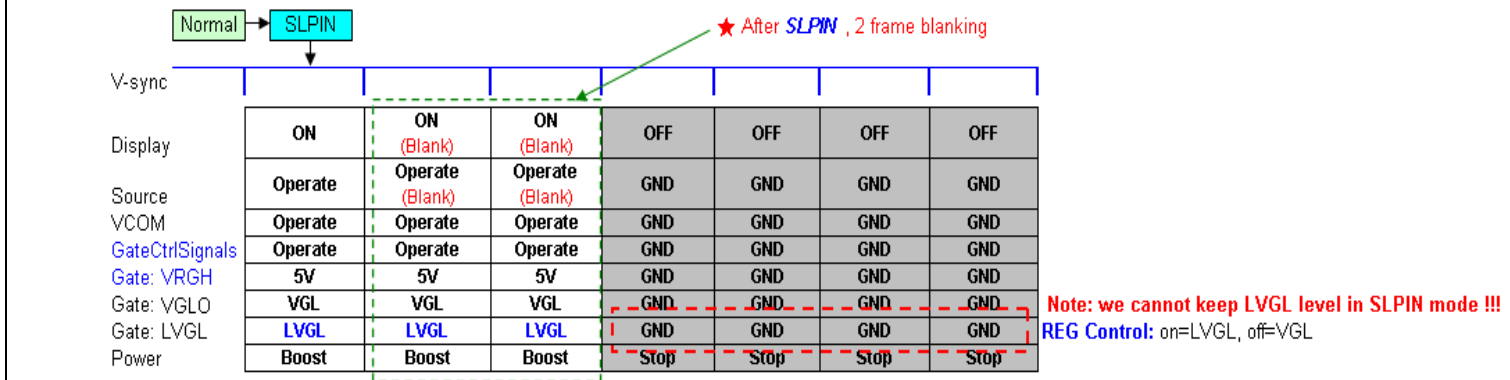
These are the “On Sequence”.



These are the “Off Sequence”.



(3) Normal → SLPIN



This is the “Abnormal Power off Sequence”.