
**A Microcoded Machine Simulator and
Microcode Assembler in a FORTH Environment**

A. Cotterman, R. Grewe, R.D. Dixon
Department of Computer Science
Wright State University

ABSTRACT

A FORTH program which provides a design tool for systems which contain a microcoded component was implemented and used in a computer architecture laboratory. The declaration of standard components such as registers, ALUs, busses, memories, and the connections is required. A sequencer and timing signals are implicit in the implementation. The microcode is written in a FORTH-like language which can be executed directly as a simulation or interpreted to produce a fixed horizontal microcode bit pattern for generating ROMs.

The direct execution of the microcode commands (rather than producing bit patterns and interpreting those instructions) gives a simpler, faster implementation. Further, the designer may concentrate on developing the design at a block level without considering some of the implementation details (such as microcode fields) which might change several times during the design cycle. However, the design is close enough to the hardware to be readily translated. Finally, the fact that the same code used for simulation may be used for assembly of the microcode instructions (after the field patterns have been specified) saves time and reduces errors.

*This paper has been submitted for publication to the **Journal of Forth Application and Research**.

